M1671

P4 Super North Bridge –

CPU, AGP, PCI and
Memory Controller

Version 0.60

M1671 : Pentium® 4 Processor, AGP, PCI and Memory Controller

Section 1 Introduction

1.1 Features

1.1.1 Processor Support

- Supports the Pentium® 4 family processors. Front side bus frequency can be up to 400 MHz.
- 64-bit data bus and 32-bit addressing
- Optimum buffering architecture design for CPU to memory, AGP and PCI read/write operations
- Flexible configured to support back to back read transfers
- Supports back to back write transfers
- Supports synchronous / pseudo asynchronous clock mode between processor and memory interface with optimized latency

1.1.2 Memory Support

- Supports SDR DRAM PC-100, PC-133
- Supports DDR up to 200, 266MHz
- Supports symmetrical and asymmetrical SDRAM / DDR addressing
- Supports 64, 128, 256, 512Mbit SDRAM / DDR
- Maximum memory size: 3GB
- Supports 6 memory rows with per byte access on each row
- Supports memory shadowing
- x-1-1-1-1-1-1-1 back-to-back page hit
- CAS before RAS and self refresh
- Pipelined SDRAM / DDR cycle control with hidden pre-charge
- Dynamic switching CKE algorithm
- Supports LVTTL(SDR)/SSTL2(DDR) signal level

1.1.3 Accelerated Graphics Port (AGP) Interface

- Supports AGP specification V2.0
- Supports up to 128 entries table look aside buffer for Graphic Address Remapping Table (GART)
- AGP 66MHz protocol
- AGP 1X/2X/4X sideband function
- 28 entries Request queue
- 64 QWORDs Read buffer
- 32 QWORDs Write buffer

1.1.4 PCI Bus Support

- Supports synchronous / asynchronous clock mode between the processor bus and the PCI bus
- 32-bit Address / Data PCI bus using PCI bus driver technology
- Supports up to 7 PCI masters excluding the M1671 and PCI-to-ISA bridge
- Parity protection on all PCI bus signals
- Fully supports PCI Configuration Space Enable (CSE) protocol
- Fully compliant with PCI Rev. 2.2
- Supports delayed transactions
- Dynamic memory prefetch algorithm and programmable post write flush algorithm
- Data Collection/Write assembly of line bursts
- Supports concurrent PCI bus burst transfers with zero wait-states
- 133 MB/sec data streaming for PCI bus to SDRAM / DDR access with minimum latency

1.1.5 Power Management

- Supports ACPI 1.0b and Legacy green
- Supports AGP Mobile BUSY# / STOP#
- Internally dynamic clock stop

1.1.6 Packaging

- 629-ball 37.5mmx37.5mm BGA package

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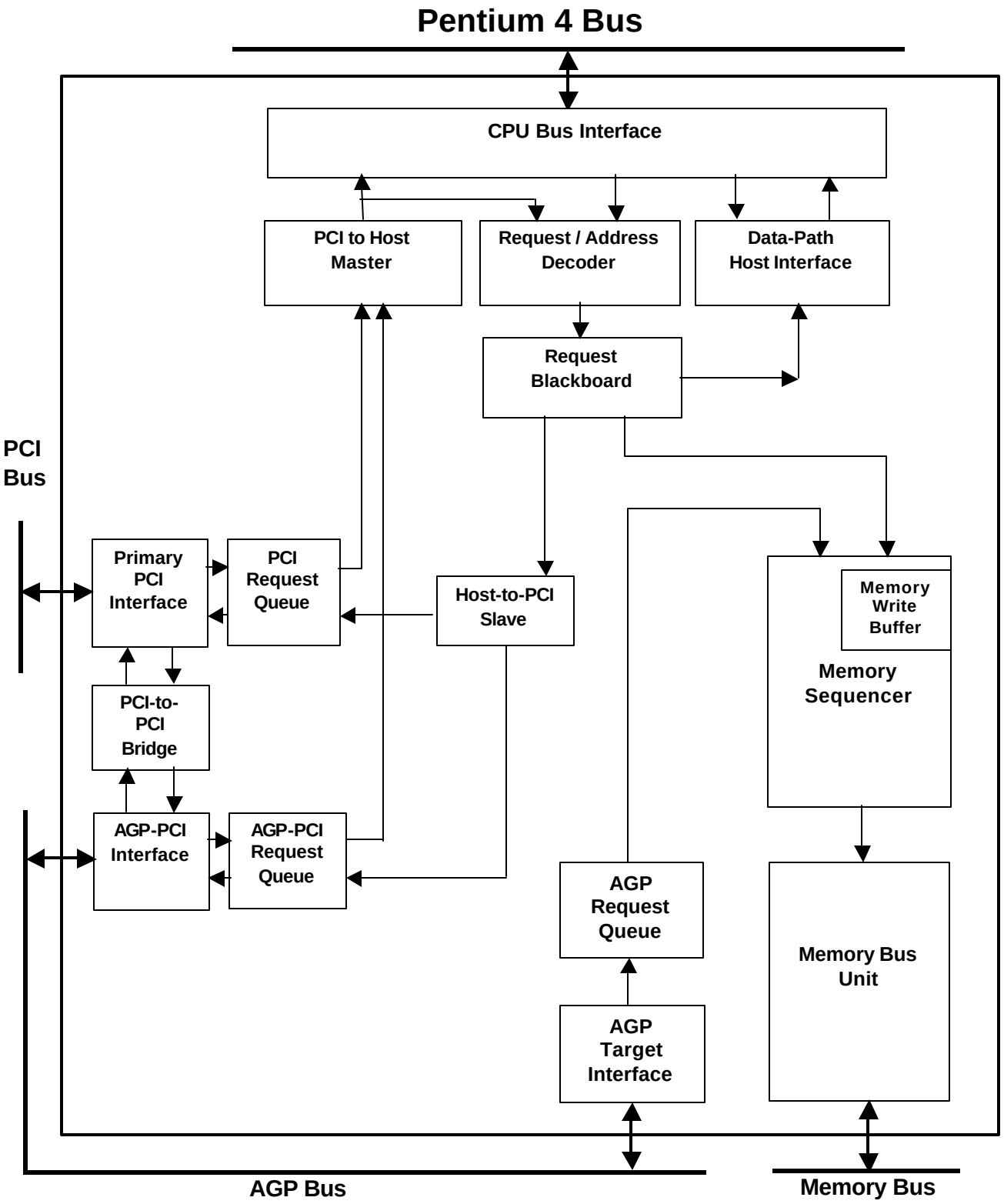

Fig.1-1 Block Diagram

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1.2 Overview

The M1671 is a high-performance, high-value North Bridge that supports all Pentium 4 processors. With internal 128-bit architecture optimized for CPU bus, DDR and AGP4X interface, the M1671 has outstanding high system performance under all types of system operations. The M1671 also has a complete set of mobile features which makes the M1671 an ideal solution for mobile systems.

The M1671 North Bridge, coupled with one of ALi's widely adopted PCI South Bridge devices (M1535, M1535D, M1535+, or M1535D+) provides a flexible and scalable motherboard core logic solution to fit all applications.

1.2.1 CPU Interface

The M1671 supports all Pentium 4 family microprocessors up to 400 MHz front side bus frequency.

1.2.2 Main Memory Interface

The M1671 can support up to 3 GB of SDRAM or DDR-SDRAM main memory with minimized internal protocol handshaking overhead. The M1671 provides a flexible system application suitable for desktop and mobile systems. In addition to dynamic memory power down, the M1671 also supports a dynamic gated clock for the internal chipset logic circuitry, which will reduce the system power consumption for mobile applications. The M1671 supports the CAS-before-RAS refresh scheme and Self-refresh scheme during normal mode and suspend mode, respectively.

1.2.3 Memory Access Control

The memory access controller plays a key role of dispatching jobs to the memory interface. By using a two-level dynamic arbitration scheme, the M1671 fulfills multiple demanding sources that need access to the main memory with minimized latency and balanced throughput. Another important role of the memory access controller is the integration logic between the AGP interface and main memory to support the AGP memory address to physical memory address translation. To fulfill this function, the M1671 uses 128 entries and 16 tags to implement a one level GART (Graphic Address Re-mapping Table) scheme.

1.2.4 AGP Interface

The M1671 supports all features of the AGP version 2.0 specification. This boosts the graphic benchmarks into another era for professional graphics usage. The M1671 design is capable of supporting 28 outstanding AGP commands (depth of command queue=28) and buffering 64QWords for AGP master read operations.

1.2.5 PCI 2.2 Compliant

The M1671 is fully compliant with the PCI 2.2 specification. Flexible PCI latency control allows the M1671 to achieve improved system performance.

1.2.6 PCI Arbiter

The M1671 PCI host interface features a flexible PCI latency controller that allows a system to be tuned for the best system performance possible. The M1671 also features an enhanced PCI arbiter that implements a fair arbitration scheme based on a PCI and CPU time slice mechanism.
In addition to itself and the South Bridge, the M1671 can support up to seven additional PCI masters. This gives designers the flexibility when deciding what combination of PCI slots and on board PCI peripheral devices to use. One of these seven PCI master channels can be assigned to a higher priority than other six PCI masters in order to fulfill the demands of some special real time devices, e.g. IEEE 1394 isochronous transmissions, when accessing main memory.

1.2.7 Power Management Design

Dark Green power management functions such as Power on Suspend, Suspend to RAM, Suspend to Disk, PCI bus CLKRUN and Dynamic Clock Stop are all supported. The M1671 provides the most flexible power management capability available in any chipset.

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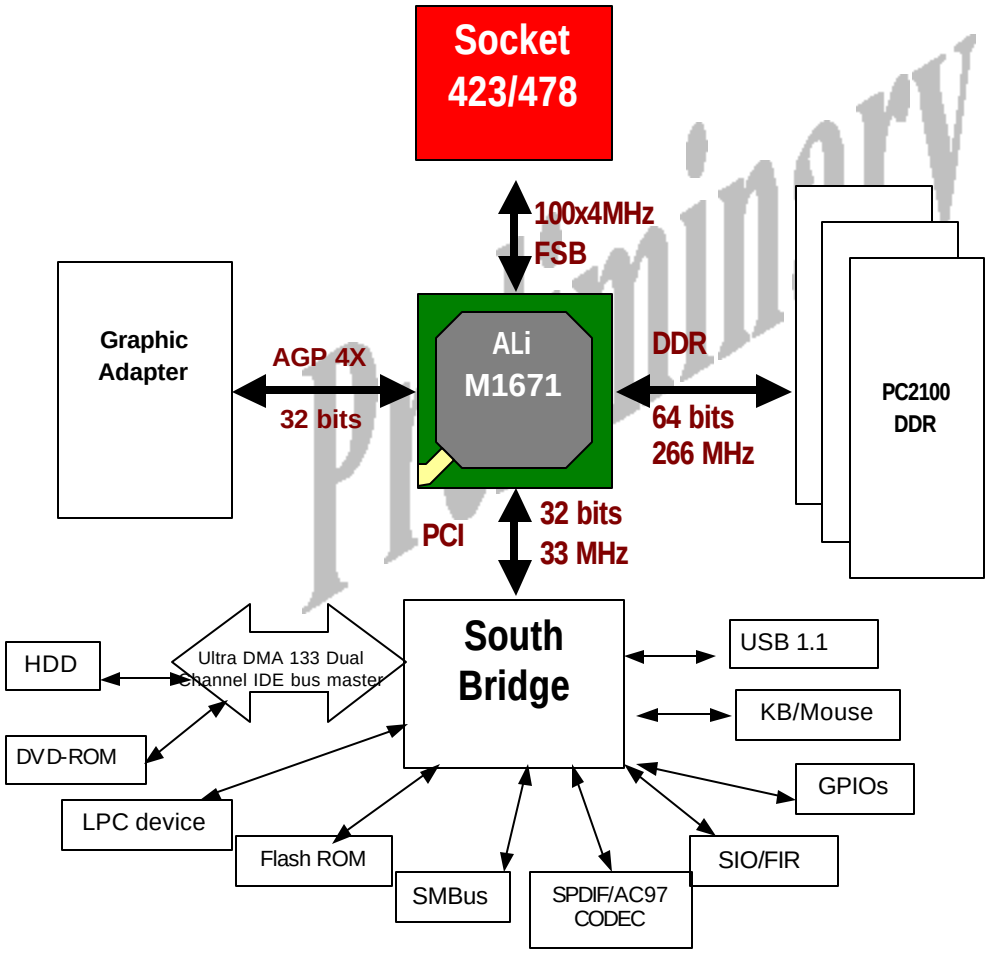
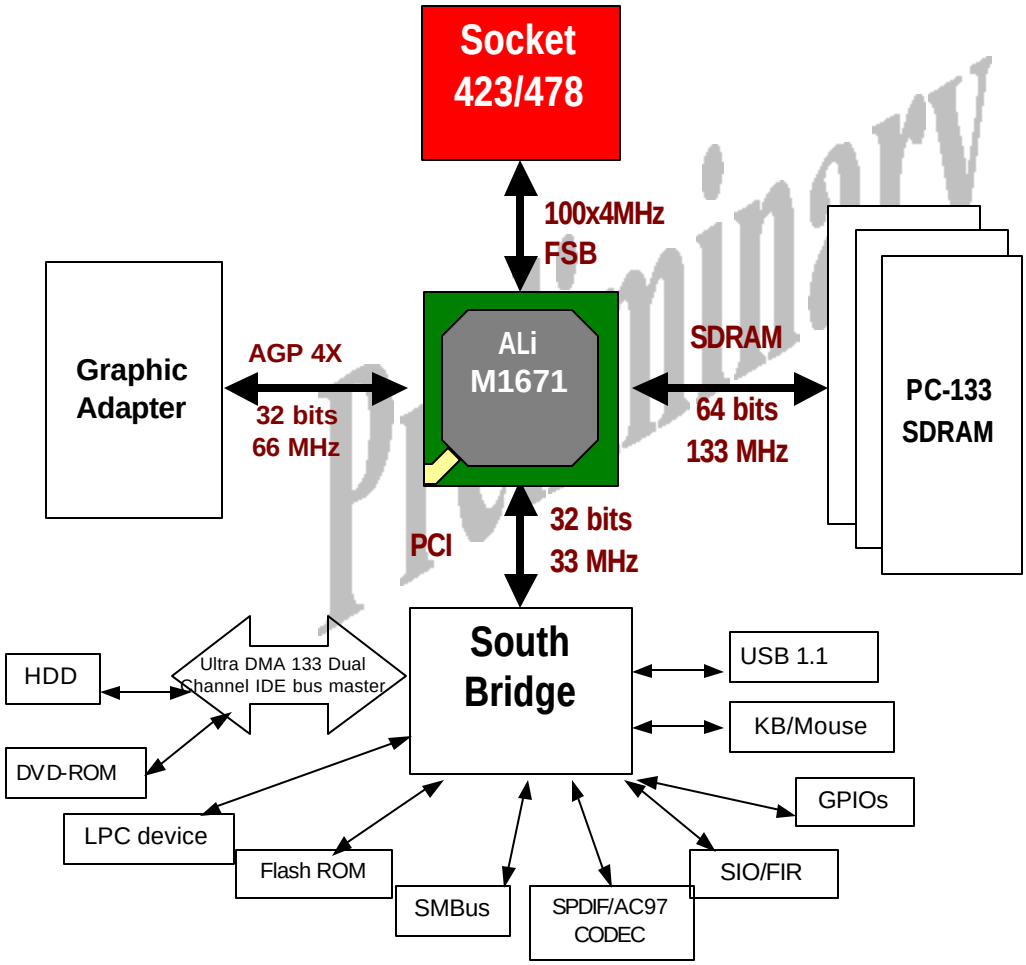
1.3 System Architecture

1.3.1 DDR Architecture



1.3.2 SDRAM Architecture



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Section 2 Pin Description

Pin Signal Description

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level.

The following notations are used to describe the signal and type

I	Input pin
O	Output pin
O/tri	Output with tri-state pin
I/O	Bi-directional pin
Analog	Analog pin
LVTTL	Low voltage TTL compatible signals
AGTL+	Assisted Gunning Transceiver Logic compatible signals
SSTL2	2.5V Small Swing Transition Level (DDR) compatible signals
AGP	Accelerated Graphics Port (AGP) compatible signals
PCI	Peripheral Component Interconnect (PCI) compatible signals
CMOS	CMOS voltage level compatible signals
P	Power
GND	Ground

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2.1 Pinout Diagram (SDR)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	PCI GND	IRDY J	AD16	AD21	AD24	AD29	REQ J1	GNT J2	GNT J3	VTT	GND	VTT	GND	HSCR HDP	A
B	DEV SELJ	TRD YJ	CBE J2	AD20	CBE J3	AD28	GNT J0	REQ J2	REQ J3	GND	VTT	GND	VTT	HSCR HDN	B
C	LOC K J	STO PJ	FRA MEJ	AD19	PCI GND	AD27	REQ J0	GNT J1	REQ J4	VTT	GND	VTT	GND	HSC RSHI	C
D	CBE J 1	PAR	SER RJ	AD18	AD23	P3A	REQ J5	REQ J6	GNT J4	GND	VTT	GND	VTT	HSCR SBP	D
E	AD14	AD15	PCI GND	AD17	P3A	AD26	AD31	GNT J5	GNT J6	VTT	GND	VTT	GND	HSCR SBN	E
F	AD11	AD12	AD13	P3A	AD22	AD25	AD30	PCI CLK	5V	GND	VTT	GND	VTT	HIG ND	F
G	AD7	AD8	CBE J0	AD9	AD10	5V									G
H	AD4	AD5	AD6	P3A	PHL DJ	PCI RSTJ									H
J	AD0	AD1	AD2	AD3	PHL DAJ	ARE QJ									J
K	GGN TJ	TYPE DETJ	AGP GND	P1A	AAG	RATI OJ									K
L	ST0	ST1	GRE QJ	SBA1	AVD DA	GCL K					P2A	P2A	VTT	VTT	L
M	RBF J	PIPE J	ST2	SBA7	SBA5	SBA3					P2A	G/T	G/T	G/T	M
N	SBA0	WBF J	AGP GND	GAD28	GAD30	AGP REF					P2A	G/T	G/T	G/T	N
P	SB_ STB	SB_S TB J	SBA2	GAD24	GAD26	P3G					G/T	G/T	G/T	G/T	P
R	SBA6	AGP GND	SBA4	P1A	GCB EJ3						G/T	G/T	G/T	G/T	R
T	GAD 29	GAD 31	AGP GND	GAD 20	GAD 22	NC					G/T	G/T	G/T	G/T	T
U	AD_S TB 1J	GAD 25	GAD 27	P1A	GAD 18	NC					P2A	G/T	G/T	G/T	U
V	GAD 23	AGP GND	AD_ STB1	GAD 16	GAD 15	NC					P2A	G/T	G/T	G/T	V
W	GAD 19	GAD 21	AGP GND	GAD 11	GAD 13	P3G					P2A	P2A	P2A	G/T	W
Y	AGP FRAM EJ	GCB EJ 2	GAD 17	P1A	GCB EJ0	GAD 9									Y
AA	AGP DEVSE LJ	AGP TRDYJ	AGPI DRYJ	GAD 2	GAD 4	GAD 6									AA
AB	AGP PAR	AGP STOPJ	AGP GND	P1A	P1A	GAD 0									AB
AC	GAD 14	GCB EJ 1	AGP SERR J	AGP SHL	AGP REF	AIGN D									AC
AD	GAD 8	GAD 10	GAD 12	AGPS ENSE	AIP OW1	AIPO W2	DRE F	CSJ5	CSJ0	SCA SJ	MA0	GND	P1B	GND	AD
AE	AD_S TB 0	AD_S TB 0J	AGP GND	P1A	SUS PEND J	DSH L	CSJ4	CSJ2	CSJ1	SRA SJ	MA1	MA2	DRE F	MA5	AE
AF	GAD 7	AGP GND	P1A	GND	CLK 32 KI	MD4	P1B	CSJ3	MD8	P1B	P1B	MD 12	P1B	MA4	AF
AG	GAD 3	GAD 5	MD0	MD 33	MD 34	GND	MD 37	MD 38	GND	MD 41	MD 11	GND	MD 45	MD 15	AG
AH	GAD 1	TEST MODE	MD 32	DQS 7	MD3	MD3 6	MD6	MD7	MD4 0	MD 10	DQS 5	MD 44	MD 14	MD 47	AH
AJ	AGP GND	TEST EN1	MD1	MD2	MD 35	MD5	DQS 6	MD 39	MD9	MD 42	MD 43	MD 13	MD 46	DQS 4	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

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(SDR-continued)

	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	GND	HD63	GND	HD57	GND	HD49	GND	HD45	GND	HD41	GND	HD35	GND	HD29	GND	A
B	HSEN SEP	HD61	HD59	HD55	HD54	HD48	HD46	HD44	HD43	HDBI 2	HD39	HD37	HD27	HD31	HD26	B
C	HSEN SEN	GND	HD56	GND	HD51	GND	HD47	GND	HD42	GND	HD38	GND	HD28	HD24	GND	C
D	HIPO W1	CPU RST	HD60	HD58	HDBI 3	HD52	HD40	HD34	HD33	HD32	HDS TBN1	HD30	GND	HDBI 1	HD25	D
E	HIPO W2	HD62	GND	HDS TBN3	GND	HD50	GND	HDS TBN2	GND	GND	GND	HDS TBP1	HD20	HD22	GND	E
F		GND	GND	HDS TBP3	HD53	HVR EF	HDV REF	HDS TBP2	HD36	GND	HD18	HD16	GND	HD17	HD21	F
G										HD14	GND	HD19	HD23	HD15	GND	G
H										HVR EF	HD11	HD10	GND	HD12	HD9	H
J										HDV REF	GND	HDS TBP0	HD3	HD8	GND	J
K										HD5	HD13	HDS TBN0	GND	HD6	HD7	K
L	VTT	VTT	VTT	VTT	VTT					GND	GND	HDBI 0	HD2	HD1	GND	L
M	G/T	G/T	P2A	P2A	VTT					GND	RSJ1	RSJ2	GND	HD4	HD0	M
N	G/T	G/T	P2A	P2A	VTT					HCV REF	GND	HLOC KJ	BPRI J	HITM J	GND	N
P	G/T	G/T	G/T	G/T	VTT					GND	DBS YJ	BRE QJ0	GND	DEF ERJ	HITJ	P
R	G/T	G/T	G/T	G/T	VTT						GND	HTRD YJ	RSJ0	BNR J	GND	R
T	G/T	G/T	G/T	G/T	VTT					GND	HRE QJ1	HRE QJ2	GND	ADSJ	DRD YJ	T
U	G/T	G/T	G/T	G/T	VTT					HA5	GND	HA4	HRE QJ4	HRE QJ3	GND	U
V	G/T	G/T	G/T	G/T	P2A					HAV REF	HA8	HAD STB0	GND	HRE QJ0	HA3	V
W	G/T	G/T	P2A	P2A	P2A					HA16	GND	HA11	HA6	HA7	GND	W
Y										GND	HA24	HA15	GND	HA9	HA10	Y
AA										HA28	GND	HA20	HA13	HA14	GND	AA
AB										HCL K+	HA30	HAD STB1	GND	HA12	HA19	AB
AC										HCL K-	GND	HA26	HA21	HA18	GND	AC
AD		MA7	MA 10	MA9	MA11	DRE F	DSH L	CKE 2	DCL K	DCL KJ	HAG	HA31	GND	HA22	HA17	AD
AE	MA3	MA8	MA 13	MA 14	MA 12	P1B	CKE 4	CKE 3	P1B	MAG	MVD DA	HVD DA	HA25	HA23	GND	AE
AF	DQM 0	P1B	MA6	DQS 3	P1B	MWE J	MD 52	P1B	CKE 5	MD 57	CKE 0	CKE 1	MD 62	HA27	HA29	AF
AG	GND	DQM 5	DQM 3	GND	MD4 9	MD 19	GND	MD5 3	MD 24	GND	MD 26	MD 28	GND	MD 31	MD 63	AG
AH	DQM 4	DQM 2	DQM 7	MD 48	MD 18	MD 51	DQS 2	MD2 2	MD 55	MD 25	MD 58	MD 59	MD 29	DQS 0	MD 30	AH
AJ	DQM 1	DQM 6	MD 16	MD 17	MD 50	MD 20	MD 21	MD 54	MD 23	MD 56	DQS 1	MD2 7	MD 60	MD 61	GND	AJ
	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

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(SDR-bottom view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
AJ	AGP GND	TEST EN1	MD1	MD2	MD 35	MD5	DQS6	MD 39	MD9	MD 42	MD 43	MD 13	MD 46	DQS4
AH	GAD1	TEST MODE	MD 32	DQS7	MD3	MD36	MD6	MD7	MD40	MD 10	DQS5	MD 44	MD 14	MD 47
AG	GAD3	GAD5	MD0	MD 33	MD 34	GND	MD 37	MD 38	GND	MD 41	MD 11	GND	MD 45	MD 15
AF	GAD7	AGP GND	P1A	GND	CLK3 2 KI	MD4	P1B	CSJ3	MD8	P1B	P1B	MD 12	P1B	MA4
AE	AD_S TB 0	AD_S TB 0J	AGP GND	P1A	SUS PEND J	DSHL	CSJ4	CSJ2	CSJ1	SRAS J	MA1	MA2	DREF	MA5
AD	GAD 8	GAD 10	GAD 12	AGPS ENSE	AIP OW1	AIPO W2	DREF	CSJ5	CSJ0	SCAS J	MA0	GND	P1B	GND
AC	GAD 14	GCB EJ 1	AGP SERRJ	AGP SHL	AGP REF	AIGN D								
AB	AGP PAR	AGP STOPJ	AGP GND	P1A	P1A	GAD0								
AA	AGP DEVSE LJ	AGP TRDYJ	AGPI DRYJ	GAD2	GAD4	GAD6								
Y	AGP FRAME J	GCB EJ 2	GAD 17	P1A	GCB EJ0	GAD9								
W	GAD1 9	GAD2 1	AGP GND	GAD1 1	GAD1 3	P3G					P2A	P2A	P2A	G/T
V	GAD2 3	AGP GND	AD_ STB1	GAD1 6	GAD1 5	NC					P2A	G/T	G/T	G/T
U	AD_S TB 1J	GAD 25	GAD 27	P1A	GAD1 8	NC					P2A	G/T	G/T	G/T
T	GAD2 9	GAD 31	AGP GND	GAD2 0	GAD2 2	NC					G/T	G/T	G/T	G/T
R	SBA6	AGP GND	SBA4	P1A	GCB EJ3						G/T	G/T	G/T	G/T
P	SB_ STB	SB_ST B J	SBA2	GAD2 4	GAD2 6	P3G					G/T	G/T	G/T	G/T
N	SBA0	WBFJ	AGP GND	GAD2 8	GAD3 0	AGP REF					P2A	G/T	G/T	G/T
M	RBFJ	PIPE J	ST2	SBA7	SBA5	SBA3					P2A	G/T	G/T	G/T
L	ST0	ST1	GRE QJ	SBA1	AVDD A	GCLK					P2A	P2A	VTT	VTT
K	GGN TJ	TYPE DETJ	AGP GND	P1A	AAG	RATI OJ								
J	AD0	AD1	AD2	AD3	PHLD AJ	ARE QJ								
H	AD4	AD5	AD6	P3A	PHLD J	PCI RSTJ								
G	AD7	AD8	CBEJ 0	AD9	AD10	5V								
F	AD11	AD12	AD13	P3A	AD22	AD25	AD30	PCI CLK	5V	GND	VTT	GND	VTT	HIGN D
E	AD14	AD15	PCI GND	AD17	P3A	AD26	AD31	GNTJ 5	GNTJ 6	VTT	GND	VTT	GND	HSCR SBN
D	CBEJ 1	PAR	SER RJ	AD18	AD23	P3A	REQJ 5	REQJ 6	GNTJ 4	GND	VTT	GND	VTT	HSCR SBP
C	LOCK J	STOP J	FRA MEJ	AD19	PCI GND	AD27	REQJ 0	GNTJ 1	REQJ 4	VTT	GND	VTT	GND	HSC RSHI
B	DEV SELJ	TRDY J	CBEJ 2	AD20	CBEJ 3	AD28	GNTJ 0	REQJ 2	REQJ 3	GND	VTT	GND	VTT	HSCR HDN
A	PCI GND	IRDY J	AD16	AD21	AD24	AD29	REQJ 1	GNTJ 2	GNTJ 3	VTT	GND	VTT	GND	HSCR HDP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

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(continued-SDR-bottom view)

15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
DQM1	DQM6	MD16	MD17	MD50	MD20	MD21	MD54	MD23	MD56	DQS1	MD27	MD60	MD61	GND	AJ
DQM4	DQM2	DQM7	MD48	MD18	MD51	DQS2	MD22	MD55	MD25	MD58	MD59	MD29	DQS0	MD30	AH
GND	DQM5	DQM3	GND	MD49	MD19	GND	MD53	MD24	GND	MD26	MD28	GND	MD31	MD63	AG
DQM0	P1B	MA6	DQS3	P1B	MWEJ	MD52	P1B	CKE5	MD57	CKE0	CKE1	MD62	HA27	HA29	AF
MA3	MA8	MA13	MA14	MA12	P1B	CKE4	CKE3	P1B	MAG	MVDDA	HVDDA	HA25	HA23	GND	AE
	MA7	MA10	MA9	MA11	DREF	DSHL	CKE2	DCLK	DCLKJ	HAG	HA31	GND	HA22	HA17	AD
									HCLK-	GND	HA26	HA21	HA18	GND	AC
									HCLK+	HA30	HADSTB1	GND	HA12	HA19	AB
									HA28	GND	HA20	HA13	HA14	GND	AA
									GND	HA24	HA15	GND	HA9	HA10	Y
G/T	G/T	P2A	P2A	P2A					HA16	GND	HA11	HA6	HA7	GND	W
G/T	G/T	G/T	G/T	P2A					HAVREF	HA8	HADSTB0	GND	HREQJ0	HA3	V
G/T	G/T	G/T	G/T	VTT					HA5	GND	HA4	HREQJ4	HREQJ3	GND	U
G/T	G/T	G/T	G/T	VTT					GND	HREQJ1	HREQJ2	GND	ADSJ	DRDYJ	T
G/T	G/T	G/T	G/T	VTT						GND	HTRDYJ	RSJ0	BNRJ	GND	R
G/T	G/T	G/T	G/T	VTT					GND	DBSYJ	BREQJ0	GND	DEFERJ	HITJ	P
G/T	G/T	P2A	P2A	VTT					HCVREF	GND	HLOCKJ	BPRIJ	HITMJ	GND	N
G/T	G/T	P2A	P2A	VTT					GND	RSJ1	RSJ2	GND	HD4	HD0	M
VTT	VTT	VTT	VTT	VTT					GND	GND	HDBI0	HD2	HD1	GND	L
									HD5	HD13	HDSTBN0	GND	HD6	HD7	K
									HDVREF	GND	HDSTBP0	HD3	HD8	GND	J
									HVREF	HD11	HD10	GND	HD12	HD9	H
									HD14	GND	HD19	HD23	HD15	GND	G
	GND	GND	HDSTBP3	HD53	HVREF	HDVREF	HDSTBP2	HD36	GND	HD18	HD16	GND	HD17	HD21	F
HIPOW2	HD62	GND	HDSTBN3	GND	HD50	GND	HDSTBN2	GND	GND	GND	HDSTBP1	HD20	HD22	GND	E
HIPOW1	CPURST	HD60	HD58	HDBI3	HD52	HD40	HD34	HD33	HD32	HDSTBN1	HD30	GND	HDBI1	HD25	D
HSENSEN	GND	HD56	GND	HD51	GND	HD47	GND	HD42	GND	HD38	GND	HD28	HD24	GND	C
HSENSEP	HD61	HD59	HD55	HD54	HD48	HD46	HD44	HD43	HDBI2	HD39	HD37	HD27	HD31	HD26	B
GND	HD63	GND	HD57	GND	HD49	GND	HD45	GND	HD41	GND	HD35	GND	HD29	GND	A
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

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(DDR-Pinout Diagram)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	PCIGND	IRDYJ	AD16	AD21	AD24	AD29	REQJ1	GNTJ2	GNTJ3	VTT	GND	VTT	GND	HSCRHDP	A
B	DEVSELJ	TRDYJ	CBEJ2	AD20	CBEJ3	AD28	GNTJ0	REQJ2	REQJ3	GND	VTT	GND	VTT	HSCRHDN	B
C	LOCKJ	STOPJ	FRAMEJ	AD19	PCIGND	AD27	REQJ0	GNTJ1	REQJ4	VTT	GND	VTT	GND	HSCRSHI	C
D	CBEJ1	PAR	SERRJ	AD18	AD23	P3A	REQJ5	REQJ6	GNTJ4	GND	VTT	GND	VTT	HSCRSBP	D
E	AD14	AD15	PCIGND	AD17	P3A	AD26	AD31	GNTJ5	GNTJ6	VTT	GND	VTT	GND	HSCRSBN	E
F	AD11	AD12	AD13	P3A	AD22	AD25	AD30	PCICLK	5V	GND	VTT	GND	VTT	HIGND	F
G	AD7	AD8	CBEJ0	AD9	AD10	5V									G
H	AD4	AD5	AD6	P3A	PHLDJ	PCIRSTJ									H
J	AD0	AD1	AD2	AD3	PHLDAJ	AREQJ									J
K	GGNTJ	TYPEDETJ	AGPGND	P1A	AAG	RATIOJ									K
L	ST0	ST1	GREQJ	SBA1	AVDDA	GCLK					P2A	P2A	VTT	VTT	L
M	RBFJ	PIPEJ	ST2	SBA7	SBA5	SBA3					P2A	G/T	G/T	G/T	M
N	SBA0	WBFJ	AGPGND	GAD28	GAD30	AGPREF					P2A	G/T	G/T	G/T	N
P	SB_STB	SB_STBJ	SBA2	GAD24	GAD26	P3G					G/T	G/T	G/T	G/T	P
R	SBA6	AGPGND	SBA4	P1A	GCBEJ3						G/T	G/T	G/T	G/T	R
T	GAD29	GAD31	AGPGND	GAD20	GAD22	NC					G/T	G/T	G/T	G/T	T
U	AD_STB1J	GAD25	GAD27	P1A	GAD18	NC					P2A	G/T	G/T	G/T	U
V	GAD23	AGPGND	AD_STB1	GAD16	GAD15	NC					P2A	G/T	G/T	G/T	V
W	GAD19	GAD21	AGPGND	GAD11	GAD13	P3G					P2A	P2A	P2A	G/T	W
Y	AGPFRAMEJ	GCBEJ2	GAD17	P1A	GCBEJ0	GAD9									Y
AA	AGPDEVSELJ	AGPTRDYJ	AGPIDRYJ	GAD2	GAD4	GAD6									AA
AB	AGPPAR	AGPSTOPJ	AGPGND	P1A	P1A	GAD0									AB
AC	GAD14	GCBEJ1	AGPSERRJ	AGPSHL	AGPREF	AIGND									AC
AD	GAD8	GAD10	GAD12	AGPSENSE	AIPOW1	AIPOW2	DVREF	CSJ4	CSJ0	MWEJ	SRASJ	GND	P1B	GND	AD
AE	AD_STB0	AD_STB0J	AGPGND	P1A	SUSPENDJ	DSHL	CSJ5	CSJ2	CSJ1	SCASJ	BA0	BA1	DVREF	A0	AE
AF	GAD7	AGPGND	P1A	GND	CLK32KI	MD60	P1B	CSJ3	MD49	P1B	P1B	MD45	P1B	A 10	AF
AG	GAD3	GAD5	MD59	MD62	MD57	GND	MD50	DM6	GND	MD46	DM5	GND	MD35	DM4	AG
AH	GAD1	TESTMODE	MD63	DQS7	MD61	MD51	MD54	MD53	MD48	MD43	DQS5	MD44	MD39	MD34	AH
AJ	AGPGND	TESTEN1	MD58	DM7	MD56	MD55	DQS6	MD52	MD47	MD42	MD41	MD40	MD38	DQS4	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

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(DDR-continued)

	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	GND	HD63	GND	HD57	GND	HD49	GND	HD45	GND	HD41	GND	HD35	GND	HD29	GND	A
B	HSEN SEP	HD61	HD59	HD55	HD54	HD48	HD46	HD44	HD43	HDBI 2	HD39	HD37	HD27	HD31	HD26	B
C	HSEN SEN	GND	HD56	GND	HD51	GND	HD47	GND	HD42	GND	HD38	GND	HD28	HD24	GND	C
D	HIPO W1	CPU RST	HD60	HD58	HDBI 3	HD52	HD40	HD34	HD33	HD32	HDS TBN1	HD30	GND	HDBI 1	HD25	D
E	HIPO W2	HD62	GND	HDS TBN3	GND	HD50	GND	HDS TBN2	GND	GND	GND	HDS TBP1	HD20	HD22	GND	E
F		GND	GND	HDS TBP3	HD53	HVR EF	HDV REF	HDS TBP2	HD36	GND	HD18	HD16	GND	HD17	HD21	F
G										HD14	GND	HD19	HD23	HD15	GND	G
H										HVR EF	HD11	HD10	GND	HD12	HD9	H
J										HDV REF	GND	HDS TBP0	HD3	HD8	GND	J
K										HD5	HD13	HDS TBN0	GND	HD6	HD7	K
L	VTT	VTT	VTT	VTT	VTT					GND	GND	HDBI 0	HD2	HD1	GND	L
M	G/T	G/T	P2A	P2A	VTT					GND	RSJ1	RSJ2	GND	HD4	HD0	M
N	G/T	G/T	P2A	P2A	VTT					HCV REF	GND	HLOC KJ	BPRI J	HITM J	GND	N
P	G/T	G/T	G/T	G/T	VTT					GND	DBS YJ	BRE QJ0	GND	DEF ERJ	HITJ	P
R	G/T	G/T	G/T	G/T	VTT						GND	HTRD YJ	RSJ0	BNR J	GND	R
T	G/T	G/T	G/T	G/T	VTT					GND	HRE QJ1	HRE QJ2	GND	ADSJ	DRD YJ	T
U	G/T	G/T	G/T	G/T	VTT					HA5	GND	HA4	HRE QJ4	HRE QJ3	GND	U
V	G/T	G/T	G/T	G/T	P2A					HAV REF	HA8	HAD STB0	GND	HRE QJ0	HA3	V
W	G/T	G/T	P2A	P2A	P2A					HA16	GND	HA11	HA6	HA7	GND	W
Y										GND	HA24	HA15	GND	HA9	HA10	Y
AA										HA28	GND	HA20	HA13	HA14	GND	AA
AB										HCL K+	HA30	HAD STB1	GND	HA12	HA19	AB
AC										HCL K-	GND	HA26	HA21	HA18	GND	AC
AD		A3	A5	A7	A9	DVR EF	DSH L	CKE 5	DCL K	DCL KJ	HAG	HA31	GND	HA22	HA17	AD
AE	A1	A2	A4	A8	A 11	P1B	CKE 4	CKE 2	P1B	MAG	MVD DA	HVD DA	HA25	HA23	GND	AE
AF	MD 37	P1B	A6	DQS 3	P1B	A12	DM 2	P1B	CKE 3	MD 13	CKE 0	CKE 1	MD 5	HA27	HA29	AF
AG	GND	MD3 2	MD 30	GND	MD 28	MD 19	GND	MD 17	MD 15	GND	MD9	MD7	GND	MD 4	MD 0	AG
AH	MD3 3	MD3 1	MD 26	MD 29	MD 24	MD 22	DQS 2	MD 16	MD 10	DM 1	MD 12	MD 3	MD 2	DQS 0	MD 1	AH
AJ	MD3 6	MD 27	DM 3	MD 25	MD 23	MD 18	MD 21	MD 20	MD 11	MD 14	DQS 1	MD8	MD 6	DM 0	GND	AJ
	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

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(DDR-bottom view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
AJ	AGP GND	TEST EN1	MD58	DM7	MD56	MD55	DQS6	MD52	MD47	MD42	MD41	MD40	MD38	DQS4
AH	GAD1	TEST MODE	MD63	DQS7	MD61	MD51	MD54	MD53	MD48	MD43	DQS5	MD44	MD39	MD34
AG	GAD3	GAD5	MD59	MD62	MD57	GND	MD50	DM6	GND	MD46	DM5	GND	MD35	DM4
AF	GAD7	AGP GND	P1A	GND	CLK32KI	MD60	P1B	CSJ3	MD49	P1B	P1B	MD45	P1B	A10
AE	AD_STB0	AD_STB0J	AGP GND	P1A	SUSPENDJ	DSHL	CSJ5	CSJ2	CSJ1	SCASJ	BA0	BA1	DVREF	A0
AD	GAD8	GAD10	GAD12	AGPSENSE	AIPOW1	AIPOW2	DVREF	CSJ4	CSJ0	MWEJ	SRASJ	GND	P1B	GND
AC	GAD14	GCBEJ1	AGPSERRJ	AGPSHL	AGPREF	AIGND								
AB	AGPPAR	AGPSTOPJ	AGP GND	P1A	P1A	GAD0								
AA	AGPDEVSELJ	AGPTRDYJ	AGPIDRYJ	GAD2	GAD4	GAD6								
Y	AGPFRAMEJ	GCBEJ2	GAD17	P1A	GCBEJ0	GAD9								
W	GAD19	GAD21	AGP GND	GAD11	GAD13	P3G					P2A	P2A	P2A	G/T
V	GAD23	AGP GND	AD_STB1	GAD16	GAD15	NC					P2A	G/T	G/T	G/T
U	AD_STB1J	GAD25	GAD27	P1A	GAD18	NC					P2A	G/T	G/T	G/T
T	GAD29	GAD31	AGP GND	GAD20	GAD22	NC					G/T	G/T	G/T	G/T
R	SBA6	AGP GND	SBA4	P1A	GCBEJ3						G/T	G/T	G/T	G/T
P	SB_STB	SB_STBJ	SBA2	GAD24	GAD26	P3G					G/T	G/T	G/T	G/T
N	SBA0	WBFJ	AGP GND	GAD28	GAD30	AGPREF					P2A	G/T	G/T	G/T
M	RBFJ	PIPEJ	ST2	SBA7	SBA5	SBA3					P2A	G/T	G/T	G/T
L	ST0	ST1	GREQJ	SBA1	AVDDA	GCLK					P2A	P2A	VTT	VTT
K	GGNTJ	TYPEDETJ	AGP GND	P1A	AAG	RATIOJ								
J	AD0	AD1	AD2	AD3	PHLDAJ	AREQJ								
H	AD4	AD5	AD6	P3A	PHLDJ	PCIRSTJ								
G	AD7	AD8	CBEJ0	AD9	AD10	5V								
F	AD11	AD12	AD13	P3A	AD22	AD25	AD30	PCICLK	5V	GND	VTT	GND	VTT	HIGND
E	AD14	AD15	PCIGND	AD17	P3A	AD26	AD31	GNTJ5	GNTJ6	VTT	GND	VTT	GND	HSCRSBN
D	CBEJ1	PAR	SERRJ	AD18	AD23	P3A	REQJ5	REQJ6	GNTJ4	GND	VTT	GND	VTT	HSCRSBP
C	LOCKJ	STOPJ	FRAMEJ	AD19	PCIGND	AD27	REQJ0	GNTJ1	REQJ4	VTT	GND	VTT	GND	HSCRSHI
B	DEVSELJ	TRDYJ	CBEJ2	AD20	CBEJ3	AD28	GNTJ0	REQJ2	REQJ3	GND	VTT	GND	VTT	HSCRHDN
A	PCIGND	IRDYJ	AD16	AD21	AD24	AD29	REQJ1	GNTJ2	GNTJ3	VTT	GND	VTT	GND	HSCRHDP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

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(continued-DDR-bottom view)

	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
AJ	MD36	MD27	DM3	MD25	MD23	MD18	MD21	MD20	MD11	MD14	DQS1	MD8	MD6	DM0	GND	AJ
AH	MD33	MD31	MD26	MD29	MD24	MD22	DQS2	MD16	MD10	DM1	MD12	MD3	MD2	DQS0	MD1	AH
AG	GND	MD32	MD30	GND	MD28	MD19	GND	MD17	MD15	GND	MD9	MD7	GND	MD 4	MD 0	AG
AF	MD37	P1B	A6	DQS3	P1B	A12	DM 2	P1B	CKE3	MD13	CKE0	CKE1	MD5	HA27	HA29	AF
AE	A1	A2	A4	A8	A11	P1B	CKE4	CKE2	P1B	MAG	MVDDA	HVDDA	HA25	HA23	GND	AE
AD		A3	A5	A7	A9	DVREF	DSHL	CKE5	DCLK	DCLKJ	HAG	HA31	GND	HA22	HA17	AD
AC										HCLK-	GND	HA26	HA21	HA18	GND	AC
AB										HCLK+	HA30	HADSTB1	GND	HA12	HA19	AB
AA										HA28	GND	HA20	HA13	HA14	GND	AA
Y										GND	HA24	HA15	GND	HA9	HA10	Y
W	G/T	G/T	P2A	P2A	P2A					HA16	GND	HA11	HA6	HA7	GND	W
V	G/T	G/T	G/T	G/T	P2A					HAVREF	HA8	HADSTB0	GND	HREQJ0	HA3	V
U	G/T	G/T	G/T	G/T	VTT					HA5	GND	HA4	HREQJ4	HREQJ3	GND	U
T	G/T	G/T	G/T	G/T	VTT					GND	HREQJ1	HREQJ2	GND	ADSJ	DRDYJ	T
R	G/T	G/T	G/T	G/T	VTT						GND	HTRDYJ	RSJ0	BNRJ	GND	R
P	G/T	G/T	G/T	G/T	VTT					GND	DBSYJ	BREQJ0	GND	DEFERJ	HITJ	P
N	G/T	G/T	P2A	P2A	VTT					HCVREF	GND	HLOCKJ	BPRIJ	HITMJ	GND	N
M	G/T	G/T	P2A	P2A	VTT					GND	RSJ1	RSJ2	GND	HD4	HD0	M
L	VTT	VTT	VTT	VTT	VTT					GND	GND	HDBI0	HD2	HD1	GND	L
K										HD5	HD13	HDSTBN0	GND	HD6	HD7	K
J										HDVREF	GND	HDSTBP0	HD3	HD8	GND	J
H										HVREF	HD11	HD10	GND	HD12	HD9	H
G										HD14	GND	HD19	HD23	HD15	GND	G
F		GND	GND	HDSTBP3	HD53	HVREF	HDVREF	HDSTBP2	HD36	GND	HD18	HD16	GND	HD17	HD21	F
E	HIPOW2	HD62	GND	HDSTBN3	GND	HD50	GND	HDSTBN2	GND	GND	GND	HDSTBP1	HD20	HD22	GND	E
D	HIPOW1	CPURST	HD60	HD58	HDBI3	HD52	HD40	HD34	HD33	HD32	HDSTBN1	HD30	GND	HDBI1	HD25	D
C	HSENSEN	GND	HD56	GND	HD51	GND	HD47	GND	HD42	GND	HD38	GND	HD28	HD24	GND	C
B	HSENSEP	HD61	HD59	HD55	HD54	HD48	HD46	HD44	HD43	HDBI2	HD39	HD37	HD27	HD31	HD26	B
A	GND	HD63	GND	HD57	GND	HD49	GND	HD45	GND	HD41	GND	HD35	GND	HD29	GND	A
	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

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2.2 Pin Description Table

Name	Type	Description
Host Interface:		
BPRI#	O GTL+	**Priority Agent**. The high priority bus agent to acquire the request bus issues Priority Agent bus request. The high priority agent will always be the next bus owner.
ADS#	I/O GTL+	**Address Strobe**. The address strobe signal is asserted during the first clock cycle request phase and indicates that address and command signals are valid.
LOCK#/ HLOCK#	I GTL+	**(Host) CPU Lock**. This LOCK# signal is asserted for indivisible sequences of transactions.
HA[31:3]	I/O GTL+	**Request Information**. HA[31:3] contain the transaction address for clock cycles with ADS# asserted. Byte Enable, deferred ID, and additional transaction information is encoded on these lines during the cycle following ADS#.
HADSTB[1:0] #	I/O GTL+	Address strobes are used to latch in HA[31:3]# and HREQ[4:0]# on their rising and falling edges.
HREQ[4:0]#	I/O GTL+	**Request Type**. HREQ[4:0]# contain the command for the clock cycles with ADS# asserted and data size/length information on the next cycle.
BREQ[0]#	O GTL+	**Bus Request 0**. Asserted during reset to set agent Ids on all processors.
BNR#	I/O GTL+	**Block Next Request** is asserted by an agent to prevent the request bus owner from issuing further requests.
HIT#	I/O GTL+	**Hit.** The bridge will assert HIT# and HITM# together to extend the snoop window of a transaction targeting its PCI bus. HIT# indicates that a caching agent holds an unmodified version of the requested line.
HITM#	I/O GTL+	**Hit Modified**. This signal indicates that a caching agent holds a modified version of the requested line and the agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
DEFER#	I/O GTL+	**DEFER#** is driven by addressed agent to indicate that the transaction cannot be guaranteed bus completion.
RS[2:0]#	O GTL+	**RS[2:0]#** encode the response to a request.
HTRDY#	O GTL+	**Host Target Ready.** Target Ready is driven by the target of the data to indicate that it is ready to receive data.
DRDY#	I/O GTL+	**Data Ready.** The data bus owner drives Data Ready for each cycle that contains valid data. DRDY# is deasserted to indicate idle cycle during data phase.
DBSY#	I/O GTL+	**DBSY#** is asserted by the data bus owner to hold the data bus for the next cycle. DBSY# is not asserted for single cycle transfers.
HD[63:0]#	I/O GTL+	**Host Data.** These signals are connected to the CPU data bus. Note that the data signals are inverted on the CPU bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.
HDBI[3:0]#	I/O GTL+	**Data Bus Inversion.** These bus signals indicate the data bus content should be inverted to get correct information. It is used to minimize the transition or active low current of CPU bus.
HDSTBP[3:0] #	I/O GTL+	**Data Strobe.** Data strobe used to latch in D[63:0]#
HDSTBN[3:0] #	I/O GTL+	**Data Strobe.** Data strobe used to latch in D[63:0]#
CPU_RST#	O GTL+	**CPU Reset.** CPU Reset is used to initialize all processor states and invalidate cache blocks without writebacks of the previous data.

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(continued)

Name	Type	Description
DRAM Interface :		
MA[12:0]	I/O LVTTL/ SSTL2	**Memory Address**, multiplexed row and column memory address. These signals are connected to the address lines of all DRAM devices. The M1671 supports SDRAM / DDR types from 64M up to 512Mbits.
BA[1:0]	I/O LVTTL/ SSTL2	**Memory Bank Address**. These signals indicate the SDRAM / DDR internal bank when accessing. These signals are connected to the bank address lines of all DRAM devices. The M1671 supports SDRAM / DDR types from 64M up to 512Mbits.
SRAS# SCAS# MWE#	I/O LVTTL/ SSTL2	**SDRAM Command**, SRAS#, SCAS# and MWE# (along with CS#) define the command being sent to the SDRAM / DDR. These signals are connected to the command lines of all DRAM devices.
CS[5:0]#	I/O LVTTL/ SSTL2	**Chip Select**. Indicates that all SDRAM / DDR commands are enabled or disabled. There is one CS# per memory row.
DQM[7:0]/ DM[7:0]	I/O LVTTL/ SSTL2	**Data Mask**. Indicates that the data byte on the bus is masked for SDRAM / DDR write cycles when asserted. Each byte lane of all memory rows shares the same DQM/DM. DQM[7]/DM[7] applied to the most significant byte, and DQM[0]/DM[0] applied to the least significant byte of every memory row.
MD[63:0]	I/O LVTTL/ SSTL2	**Memory Data**. These signals are connected to the DRAM data bus. MD[63] is the most significant bit and MD[0] is the least significant bit.
CKE[5:0]	I/O LVTTL	**Clock Enable**. Clock enable for the SDRAM / DDR to perform a self refresh cycle. This signal should be asserted when the system is idle and the gated function is enabled.
DQS[7:0]	I/O SSTL2	**Data Strobe**. Indicates the relative edge-sampling time frame of the DDR data transaction. (DDR only)
AGP Interface :		
PIPE#	I AGP 1x	**Pipeline Request** is asserted by a master to indicate a full width request to be en-queued by the target. The target en-queues one request for each rising edge of AGP clock while PIPE# is asserted. When PIPE# is de-asserted, no new requests are en-queued across GAD bus.
SBA[7:0]	I/O-AGP 1x/2x/4x	**Sideband Address port** provides an additional bus to pass address and commands to the target from the master.
RBF#	I AGP 1x	**Read Buffer Full**, indicated if the master is ready to accept previously requested low priority read data. When RBF# is asserted, the arbiter is not allowed to initiate the return of low priority read data to the master.
WBF#	I AGP 1x	**Write Buffer Full** indicates if the master is ready to accept FastWrite data from the core-logic. When WBF# is asserted, the core-logic arbiter is not allowed to initiate a transaction to provide FastWrite data.
ST[2:0]	I/O AGP 1x	**Status Bus** provides information from the arbiter to a Master on what it may do. Refer to AGP Spec. 2.0 for details.
AD_STB0	I/O AGP 2x/4x	**Address Bus Strobe 0.** Address Bus Strobe 0 provides strobe timing for the 2x/4x data transfer mode on the GAD[15:0] signals. The agent that is providing data drives this signal.
AD_STB0#	I/O AGP 2x/4x	**Address Bus Strobe0#.** Address Bus Strobe 0# compliments and AD_STB0# provides timing for the 4x data transfer mode on GAD[15:0] signals. The agent that is providing data drives this signal.
AD_STB1	I/O AGP 2x/4x	**Address Bus Strobe 1.** Address Bus Strobe 1 provides strobe timing for the 2x/4x data transfer mode on the GAD[31:16]. The agent that is providing data drives this signal.
AD_STB1#	I/O AGP 2x/4x	**Address Bus Strobe 1#.** Address Bus Strobe 1# compliments and AD_STB1# provides timing for the 4x data transfer mode on GAD[31:16]. The agent that is providing data drives this signal.
SB_STB	I AGP 2x/4x	**Side Band Strobe** provides strobe timing for SBA[7:0] and is always driven by the AGP master.
SB_STB#	I, AGP 2x/4x	**Side Band Strobe** compliment and SB_STB# provide timing for SBA[7:0] (when supported) when the 4x timing is supported and is always driven by the AGP master.

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(continued)

Name	Type	Description
AGP Semantics PCI Signals:		
GFRAME#	I/O AGP 1x	**AGP Frame.** AGP Frame is driven by a master to indicate the beginning and duration of a transaction. Not used by AGP cycle. It remains de-asserted by its own pull up resistor.
GIRDY#	I/O AGP 1x	**GIRDY#** indicates the AGP compliant master is ready to provide all write data for the current transaction. Once GIRDY# is asserted for a write operation, the master is not allowed to insert wait states. The assertion of GIRDY# for reads, indicates that the master is ready to transfer a subsequent block of read data.
GTRDY#	I/O AGP 1x	**GTRDY#** indicates the AGP compliant target is ready to provide read data for the entire transaction or is ready to transfer a block of data, when the transfer requires more than four clocks to complete.
GSTOP#	I/O AGP 1x	**GSTOP#** is a request from the target to stop the current transaction.
GDEVSEL#	I/O AGP 1x	**Device Select**. The device that has decoded its address as the target of the current access drives Device Select.
GSERR#	I AGP 1x	**AGP System Error**. This signal is used to report a catastrophic error to the system by the devices on the AGP bus.
GREQ#	I-AGP1x	**GREQ#** is used to request access to the bus to initiate a PCI or an AGP request.
GGNT#	I/O AGP 1x	**GGNT#** provides additional information on ST[2:0]. The additional information indicates that the master is the recipient of previously requested read data, it is to provide write data, for a previously en-queued write command or has been given permission to start a bus transaction.
GAD[31:0]	I/O-AGP 1x/2x/4x	**GAD[31:0]** is the multiplexed address and data transfer bus. GAD[31] is the most significant bit and GAD[0] is the least significant bit.
GCBE[3:0]#	I/O AGP 1x/2x/4x	**GCBE[3:0]#** are the multiplexed command and byte enable bus. They also provide command information by the master when requests are being en-queued using PIPE#. Provides valid byte information during AGP write transactions and is driven by the master.
GPAR	I/O AGP 1x	**GPAR** is parity bit on GAD[31:0] and GCBE[3:0]#.
TYPEDET#	I AGP 1x	**AGP** 2x or 4x type detect mode active low signal.
PCI Interface:		
AD[31:0]	I/O PCI	**PCI Address and Data.** These signals contain the address or data for PCI transaction, and connect to the PCI bus.
CBE[3:0]#	I/O PCI	**PCI Bus Command and Byte Enables.** These signals contain command during address phase and byte enables during the data phase.
FRAME#	I/O PCI	**PCI Frame** is driven by a master to indicate the beginning and duration of a transaction.
DEVSEL#	I/O PCI	The device that has decoded its address as the target of the current access drives **Device Select**.
IRDY#	I/O PCI	**PCI Initiator Ready** is asserted by the master to indicate that it is able to complete the current data transfer. A data transfer occurs if both PTRDY# and IRDY# are asserted during the rising edge of PCICLK.
PTRDY#	I/O PCI	**PCI Target Ready.** This signal is asserted by the target to indicate that it is able to complete the current data transfer. A data transfer occurs if PTRDY# and IRDY# are asserted during the rising edge of PCICLK.
STOP#	I/O-PCI	**STOP#** is a request from the target to stop the current transaction.
PLOCK#	I/O-PCI	**PCI Lock** is asserted by the agent requiring exclusive access to target.
PAR	I/O PCI	**PCI Parity** is driven to even parity across AD[31:0] and CBE[3:0]# by the master during the address and write data phase. The target drives parity during read data phase.
SERR# / CLKRUN#	I/O PCI	**PCI System Error.** This signal is used to report a catastrophic error to the system by devices on the PCI bus.

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(continued)

Name	Type	Description
PCI Sideband/Bridge Interface:		
PHLD#	I PCI	**PCI Hold#**. This signal comes from the standard bus bridge (South Bridge) to PCI arbiter to request the PCI bus.
PHLDA#	I/O PCI	**PCI Hold Acknowledge#.** This signal is driven by the internal PCI arbiter to grant the PCI bus to the standard bus bridge (South Bridge).
PREQ[6:0]#/ AGP_BUSY#	I PCI	**Request.** PCI master requests for PCI slots or on board PCI device. AGP_BUSY# / STP_AGP# protocol supporting ACPI between AGP device and M1671 is muxed with PCI master request channel 5. (Reference configuration register index 4Ah.)
PGNT[6:0]#/ STP_AGP#	I/O PCI	**Grant**. Permission is given to the PCI master to use the PCI bus. These are inputs when the test mode is enabled. These pins are required to be external pull high. AGP_BUSY# /STP_AGP# protocol supporting ACPI between AGP device and M1671 is muxed with PCI master grant channel 5. (Reference configuration register index 4Ah.)
AREQ#	I/O PCI	**Any Request** represents bus request of any PCI bus masters. As output, this signal will be asserted by the M1671 when any PREQ[5:0]# or GREQ# has been asserted. It is used to connect to the south bridge to support ACPI function.
Clocks :		
HCLK+ HCLK-	I CMOS	**Host Bus Interface Clock**. This is the Host (CPU) bus interface clock input.
DCLK+ DCLK-	I CMOS/ SSTL2	**DRAM Bus Interface Clock.** This is the SDRAM/DDR interface clock input. When in the SDRAM mode, only the DCLK+ input is recognized. When in the DDR mode, both DCLK+, DCLK- input is treated as differential clock inputs following the SSTL2 signal specification.
GCLKI	I LVTTL	**AGP Bus Interface Clock.** This is the AGP interface clock input which is generated by the clock generator and must lag HCLK 1~3 ns.
PCICLK	I LVTTL	**PCI Bus interface reference Clock**. This is the PCI interface reference clock input which is generated by the clock generator and must lag HCLK 1~3 ns.
CLK32KI	I LVTTL	**32KHz Clock** for suspend to DRAM refresh. This signal must be pulled to a fixed value when the suspend feature is disabled.
Miscellaneous :		
SUSPEND#	I LVTTL	**Suspend Request**. This request comes from a south bridge. When sampled active, the M1671 will enter the DRAM suspend refresh state. This signal must be pulled high when the suspend feature is disabled.
RATIO#	O LVTTL	**Ratio.** The M1671 will connect this signal to external circuitry to add the CPU configuration latch hold time.
RESET#	I LVTTL	**System Reset.** This reset is from the system. The M1671 will reset the whole state machine and generate CPU_RST# to the CPU.
TEST_MODE	I LVTTL	**Internal Test Mode.** This input is used to enable the internal scan test.
NT_TEST_EN	I LVTTL	**NAND Tree Test Mode Enable.** This input is used to enable the NAND tree test mode.
HAVREF HCVREF HDVREF	P	**Host Reference Voltage.** System designers must provide a stable reference voltage input to work reliably.
DVREF	P	**DDR Reference Voltage.** System designers must provide a stable 1.25V input to this signal for reliable operation when using DDR for the system memory. When using SDRAM as the system memory, tie these pins low. Total of 3 balls.
AGPVREF	P	**AGP Reference Voltage.** These inputs are used for the AGP pad reference input. Total of 2 balls. (1.32V/0.75V) 0.4*3.3V if DETECT#: High 0.5*1.5V if DETECT#: GND

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(continued)

Name	Type	Description
HVREFSHL	GND	**CPU Reference Voltage Shielding.** These inputs provide shielding for the GTL reference voltage.
DSHL	GND	**DDR Reference Voltage Shielding.** These inputs provide shielding for the DDR reference voltage.
AGPSHL	GND	**AGP Reference Voltage Shielding.** These inputs provide shielding for the AGP reference voltage.
HSENSEP	Analog	**Host Impedance Sense** for termination.
HSENSEN	Analog	**Host Impedance Sense** for driving strength.
HSCRHDP HSCRSBP	Analog	**Host Bus Slew Rate Control (1V).**
HSCRHDN HSCRSBN	Analog	**Host Bus Slew Rate Control (1.25V).**
AGPSENSE	Analog	**AGP Impedance Sense.**
Power & Ground :		
HVDDA	P	**2.5V**. Power for the internal Host PLL analog core.
HAG	GND	**Ground** for the internal Host PLL analog core.
MVDDA	P	**2.5V**. Power for the internal Memory PLL analog core.
MAG	GND	**Ground** for the internal Memory PLL analog core.
AVDDA	P	**2.5V**. Power for the internal AGP PLL analog core.
AAG	GND	**Ground**. Ground for the internal Memory PLL Analog core.
HIPOW1	P	**Power** for the Host impedance matching circuitry. (CPU Vcore 1.1V~1.85V)
HIPOW2	P	**2.5V**. Power for the Host impedance matching circuitry.
HIGND	GND	**Ground**. Ground for the HIPOW1&2 circuitry.
AIPOW1	P	**1.5V/3.3V.** Power for the AGP impedance matching circuitry.
AIPOW2	P	**2.5V.** Power for the AGP impedance matching circuitry.
AIGND	GND	**Ground**. Ground for the AIPOW1&2 circuitry.
PCI_5V	P	**5V.** Power for 5V tolerance on the PCI interface. Total of 2 balls.
VTT	P	**I/O power** for the AGTL bus. Total 25 balls. (CPU Vcore 1.1V~1.85V)
P1A	P	**3.3V/1.5V**. I/O power for the AGP bus. Total 8 balls.
P1B	P	**3.3V/2.5V**. I/O power for the Memory interface. Total 10 balls.
P3A	P	**3.3V**. I/O power for the PCI interface. Total 4 balls.
P3G	P	**3.3V**. I/O pre-drive power for the AGP bus. Total 2 balls.
P2A	P	**2.5V**. Core power for the core logic. Total 17 balls.
GND	GND	**Ground**.
G/T	GND	**Ground/Thermal**.

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2.3 Multiplexed Pin Signal Definition

Register Setting	M1671 index register								
	Ball Out	76h [2:0] = 000b	76h [2:0] = 1xxb	Ball Out	76h[2:0] = 000b	76h[2:0] = 1xx b	Ball Out	76h [2:0] = 000b	76h [2:0] = 1xx b
		SDRAM	**DDR**		**SDRAM**	**DDR**		**SDRAM**	**DDR**
Signal Name	AF23	CKE5	CKE3	AG10	MD41	MD46	AJ16	DQM6	MD27
	AE22	CKE3	CKE2	AG11	MD11	DM5	AJ17	MD16	DM3
	AD8	CS5#	CS4#	AG13	MD45	MD35	AJ18	MD17	MD25
	AD10	SCAS#	MWE#	AG14	MD15	DM4	AJ19	MD50	MD23
	AD11	MA0	SRAS#	AG16	DQM5	MD32	AJ20	MD20	MD18
	AD16	MA7	MA3	AG17	DQM3	MD30	AJ22	MD54	MD20
	AD17	MA10	MA5	AG19	MD49	MD28	AG23	MD24	MD15
	AD18	MA9	MA7	AG22	MD53	MD17	AF24	MD57	MD13
	AD19	MA11	MA9	AJ24	MD56	MD14	AG25	MD26	MD9
	AF27	MD62	MD5	AH26	MD59	MD3			
	AG28	MD31	MD4	AH3	MD32	MD63			
	AG29	MD63	MD0	AH5	MD3	MD61			
	AE7	CS4#	CS5#	AH6	MD36	MD51			
	AE10	SRAS#	SCAS#	AH7	MD6	MD54			
	AE11	MA1	BA0	AH8	MD7	MD53			
	AE12	MA2	BA1	AH9	MD40	MD48			
	AE14	MA5	MA0	AH10	MD10	MD43			
	AE15	MA3	MA1	AH13	MD14	MD39			
	AE16	MA8	MA2	AH14	MD47	MD34			
	AE17	BA0	MA4	AH15	DQM4	MD33			
	AE18	BA1	MA8	AH16	DQM2	MD31			
	AE19	MA12	MA11	AH17	DQM7	MD26			
	AD22	CKE2	CKE5	AH18	MD48	MD29			
	AJ28	MD61	DM0	AH19	MD18	MD24			
	AH29	MD30	MD1	AH20	MD51	MD22			
	AF6	MD4	MD60	AH22	MD22	MD16			
	AF9	MD8	MD49	AH23	MD55	MD10			
	AF12	MD12	MD45	AH24	MD25	DM1			
	AF14	MA4	MA10	AH25	MD58	MD12			
	AF15	DQM0	MD37	AJ26	MD27	MD8			
	AF20	MWE#	MA12	AJ3	MD1	MD58			
	AF21	MD52	DM2	AJ4	MD2	DM7			
	AJ23	MD23	MD11	AJ5	MD35	MD56			
	AG26	MD28	MD7	AJ6	MD5	MD55			
	AJ27	MD60	MD6	AJ8	MD39	MD52			
	AH27	MD29	MD2	AJ9	MD9	MD47			
	AG3	MD0	MD59	AJ10	MD42	MD42			
	AG4	MD33	MD62	AJ11	MD43	MD41			
	AG5	MD34	MD57	AJ12	MD13	MD40			
	AG7	MD37	MD50	AJ13	MD46	MD38			
	AG8	MD38	DM6	AJ15	DQM1	MD36			

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2.4 Numerical Pin List (SDR)

Pin No.	Pin Name
A1	PCIGND
A2	IRDYJ
A3	AD16
A4	AD21
A5	AD24
A6	AD29
A7	REQJ1
A8	GNTJ2
A9	GNTJ3
A10	VTT
A11	GND
A12	VTT
A13	GND
A14	HSCRHDP
A15	GND
A16	HD63
A17	GND
A18	HD57
A19	GND
A20	HD49
A21	GND
A22	HD45
A23	GND
A24	HD41
A25	GND
A26	HD35
A27	GND
A28	HD29
A29	GND
B1	DEVSELJ
B2	TRDYJ
B3	CBEJ2
B4	AD20
B5	CBEJ3
B6	AD28
B7	GNTJ0
B8	REQJ2
B9	REQJ3
B10	GND
B11	VTT
B12	GND
B13	VTT
B14	HSCRHDN
B15	HSENSEP
B16	HD61
B17	HD59
B18	HD55
B19	HD54
B20	HD48
B21	HD46

Pin No.	Pin Name
B22	HD44
B23	HD43
B24	HDBI2
B25	HD39
B26	HD37
B27	HD27
B28	HD31
B29	HD26
C1	PLOCKJ
C2	STOPJ
C3	FRAMEJ
C4	AD19
C5	PCIGND
C6	AD27
C7	REQJ0
C8	GNTJ1
C9	REQJ4
C10	VTT
C11	GND
C12	VTT
C13	GND
C14	HSCRSHI
C15	HSENSEN
C16	GND
C17	HD56
C18	GND
C19	HD51
C20	GND
C21	HD47
C22	GND
C23	HD42
C24	GND
C25	HD38
C26	GND
C27	HD28
C28	HD24
C29	GND
D1	CBEJ1
D2	PAR
D3	SERRJ
D4	AD18
D5	AD23
D6	P3A
D7	REQJ5
D8	REQJ6
D9	GNTJ4
D10	GND
D11	VTT
D12	GND
D13	VTT

Pin No.	Pin Name
D14	HSCRSBP
D15	HIPOW1
D16	CPURST
D17	HD60
D18	HD58
D19	HDBI3
D20	HD52
D21	HD40
D22	HD34
D23	HD33
D24	HD32
D25	HDSTBN1
D26	HD30
D27	GND
D28	HDBI1
D29	HD25
E1	AD14
E2	AD15
E3	PCIGND
E4	AD17
E5	P3A
E6	AD26
E7	AD31
E8	GNTJ5
E9	GNTJ6
E10	VTT
E11	GND
E12	VTT
E13	GND
E14	HSCRSBN
E15	HIPOW2
E16	HD62
E17	GND
E18	HDSTBN3
E19	GND
E20	HD50
E21	GND
E22	HDSTBN2
E23	GND
E24	GND
E25	GND
E26	HDSTBP1
E27	HD20
E28	HD22
E29	GND
F1	AD11
F2	AD12
F3	AD13
F4	P3A
F5	AD22

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(SDR-continued)

Pin No.	Pin Name
F6	AD25
F7	AD30
F8	PCICLK
F9	5V
F10	GND
F11	VTT
F12	GND
F13	VTT
F14	HIGND
F16	GND
F17	GND
F18	HDSTBP3
F19	HD53
F20	HVREFSHL
F21	HDVREF
F22	HDSTBP2
F23	HD36
F24	GND
F25	HD18
F26	HD16
F27	GND
F28	HD17
F29	HD21
G1	AD7
G2	AD8
G3	CBEJ0
G4	AD9
G5	AD10
G6	5V
G24	HD14
G25	GND
G26	HD19
G27	HD23
G28	HD15
G29	GND
H1	AD4
H2	AD5
H3	AD6
H4	P3A
H5	PHLDJ
H6	PCIRSTJ
H24	HVREFSHL
H25	HD11
H26	HD10
H27	GND
H28	HD12
H29	HD9
J1	AD0
J2	AD1
J3	AD2

Pin No.	Pin Name
J4	AD3
J5	PHLDAJ
J6	AREQJ
J24	HDVREF
J25	GND
J26	HDSTBP0
J27	HD3
J28	HD8
J29	GND
K1	GGNTJ
K2	TYPEDETJ
K3	AGPGND
K4	P1A
K5	AAG
K6	RATIOJ
K24	HD5
K25	HD13
K26	HDSTBN0
K27	GND
K28	HD6
K29	HD7
L1	ST0
L2	ST1
L3	GREQJ
L4	SBA1
L5	AVDDA
L6	GCLK
L11	P2A
L12	P2A
L13	VTT
L14	VTT
L15	VTT
L16	VTT
L17	VTT
L18	VTT
L19	VTT
L24	GND
L25	GND
L26	HDBI0
L27	HD2
L28	HD1
L29	GND
M1	RBFJ
M2	PIPEJ
M3	ST2
M4	SBA7
M5	SBA5
M6	SBA3
M11	P2A
M12	G/T

Pin No.	Pin Name
M13	G/T
M14	G/T
M15	G/T
M16	G/T
M17	P2A
M18	P2A
M19	VTT
M24	GND
M25	RSJ1
M26	RSJ2
M27	GND
M28	HD4
M29	HD0
N1	SBA0
N2	WBFJ
N3	AGPGND
N4	GAD28
N5	GAD30
N6	AGPREF
N11	P2A
N12	G/T
N13	G/T
N14	G/T
N15	G/T
N16	G/T
N17	P2A
N18	P2A
N19	VTT
N24	HCVREF
N25	GND
N26	HLOCKJ
N27	BPRIJ
N28	HITMJ
N29	GND
P1	SB_STB
P2	SB_STBJ
P3	SBA2
P4	GAD24
P5	GAD26
P6	P3G
P11	G/T
P12	G/T
P13	G/T
P14	G/T
P15	G/T
P16	G/T
P17	G/T
P18	G/T
P19	VTT
P24	GND

(SDR-continued)

Pin No.	Pin Name
P25	DBSYJ
P26	BREQJ0
P27	GND
P28	DEFERJ
P29	HITJ
R1	SBA6
R2	AGPGND
R3	SBA4
R4	P1A
R5	GCBEJ3
R11	G/T
R12	G/T
R13	G/T
R14	G/T
R15	G/T
R16	G/T
R17	G/T
R18	G/T
R19	VTT
R25	GND
R26	HTRDYJ
R27	RSJ0
R28	BNRJ
R29	GND
T1	GAD29
T2	GAD31
T3	AGPGND
T4	GAD20
T5	GAD22
T6	NC
T11	G/T
T12	G/T
T13	G/T
T14	G/T
T15	G/T
T16	G/T
T17	G/T
T18	G/T
T19	VTT
T24	GND
T25	HREQJ1
T26	HREQJ2
T27	GND
T28	ADSJ
T29	DRDYJ
U1	AD_STB1J
U2	GAD25
U3	GAD27
U4	P1A
U5	GAD18

Pin No.	Pin Name
U6	NC
U11	P2A
U12	G/T
U13	G/T
U14	G/T
U15	G/T
U16	G/T
U17	G/T
U18	G/T
U19	VTT
U24	HA5
U25	GND
U26	HA4
U27	HREQJ4
U28	HREQJ3
U29	GND
V1	GAD23
V2	AGPGND
V3	AD_STB1
V4	GAD16
V5	GAD15
V6	NC
V11	P2A
V12	G/T
V13	G/T
V14	G/T
V15	G/T
V16	G/T
V17	G/T
V18	G/T
V19	P2A
V24	HAVREF
V25	HA8
V26	HADSTB0
V27	GND
V28	HREQJ0
V29	HA3
W1	GAD19
W2	GAD21
W3	AGPGND
W4	GAD11
W5	GAD13
W6	P3G
W11	P2A
W12	P2A
W13	P2A
W14	G/T
W15	G/T
W16	G/T
W17	P2A

Pin No.	Pin Name
W18	P2A
W19	P2A
W24	HA16
W25	GND
W26	HA11
W27	HA6
W28	HA7
W29	GND
Y1	AGPFRAMEJ
Y2	GCBEJ2
Y3	GAD17
Y4	P1A
Y5	GCBEJ0
Y6	GAD9
Y24	GND
Y25	HA24
Y26	HA15
Y27	GND
Y28	HA9
Y29	HA10
AA1	AGPDEVSELJ
AA2	AGPTRDYJ
AA3	AGPIRDYJ
AA4	GAD2
AA5	GAD4
AA6	GAD6
AA24	HA28
AA25	GND
AA26	HA20
AA27	HA13
AA28	HA14
AA29	GND
AB1	AGPPAR
AB2	AGPSTOPJ
AB3	AGPGND
AB4	P1A
AB5	P1A
AB6	GAD0
AB24	HCLK+
AB25	HA30
AB26	HADSTB1
AB27	GND
AB28	HA12
AB29	HA19
AC1	GAD14
AC2	GCBEJ1
AC3	AGPSERRJ
AC4	AGPSHL
AC5	AGPREF
AC6	AIGND

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(SDR-continued)

Pin No.	Pin Name
AC24	HCLK-
AC25	GND
AC26	HA26
AC27	HA21
AC28	HA18
AC29	GND
AD1	GAD8
AD2	GAD10
AD3	GAD12
AD4	AGPSENSE
AD5	AIPOW1
AD6	AIPOW2
AD7	DREF
AD8	CSJ5
AD9	CSJ0
AD10	SCASJ
AD11	MA0
AD12	GND
AD13	P1B
AD14	GND
AD16	MA7
AD17	MA10
AD18	MA9
AD19	MA11
AD20	DREF
AD21	DSHL
AD22	CKE2
AD23	DCLK
AD24	DCLKJ
AD25	HAG
AD26	HA31
AD27	GND
AD28	HA22
AD29	HA17
AE1	AD_STB0
AE2	AD_STB0J
AE3	AGPGND
AE4	P1A
AE5	SUSPENDJ
AE6	DSHL
AE7	CSJ4
AE8	CSJ2
AE9	CSJ1
AE10	SRASJ
AE11	MA1
AE12	MA2
AE13	DREF
AE14	MA5
AE15	MA3
AE16	MA8

Pin No.	Pin Name
AE17	BA0
AE18	BA1
AE19	MA12
AE20	P1B
AE21	CKE4
AE22	CKE3
AE23	P1B
AE24	MAG
AE25	MVDDA
AE26	HVDDA
AE27	HA25
AE28	HA23
AE29	GND
AF1	GAD7
AF2	AGPGND
AF3	P1A
AF4	GND
AF5	CLK32KI
AF6	MD4
AF7	P1B
AF8	CSJ3
AF9	MD8
AF10	P1B
AF11	P1B
AF12	MD12
AF13	P1B
AF14	MA4
AF15	DQM0
AF16	P1B
AF17	MA6
AF18	DQS3
AF19	P1B
AF20	MWEJ
AF21	MD52
AF22	P1B
AF23	CKE5
AF24	MD57
AF25	CKE0
AF26	CKE1
AF27	MD62
AF28	HA27
AF29	HA29
AG1	GAD3
AG2	GAD5
AG3	MD0
AG4	MD33
AG5	MD34
AG6	GND
AG7	MD37
AG8	MD38

Pin No.	Pin Name
AG9	GND
AG10	MD41
AG11	MD11
AG12	GND
AG13	MD45
AG14	MD15
AG15	GND
AG16	DQM5
AG17	DQM3
AG18	GND
AG19	MD49
AG20	MD19
AG21	GND
AG22	MD53
AG23	MD24
AG24	GND
AG25	MD26
AG26	MD28
AG27	GND
AG28	MD31
AG29	MD63
AH1	GAD1
AH2	TESTMODE
AH3	MD32
AH4	DQS7
AH5	MD3
AH6	MD36
AH7	MD6
AH8	MD7
AH9	MD40
AH10	MD10
AH11	DQS5
AH12	MD44
AH13	MD14
AH14	MD47
AH15	DQM4
AH16	DQM2
AH17	DQM7
AH18	MD48
AH19	MD18
AH20	MD51
AH21	DQS2
AH22	MD22
AH23	MD55
AH24	MD25
AH25	MD58
AH26	MD59
AH27	MD29
AH28	DQS0
AH29	MD30

(SDR-continued)

Pin No.	Pin Name
AJ1	AGPGND
AJ2	TESTEN1
AJ3	MD1
AJ4	MD2
AJ5	MD35
AJ6	MD5
AJ7	DQS6
AJ8	MD39
AJ9	MD9
AJ10	MD42
AJ11	MD43
AJ12	MD13
AJ13	MD46
AJ14	DQS4
AJ15	DQM1
AJ16	DQM6
AJ17	MD16
AJ18	MD17
AJ19	MD50
AJ20	MD20
AJ21	MD21
AJ22	MD54
AJ23	MD23
AJ24	MD56
AJ25	DQS1
AJ26	MD27
AJ27	MD60
AJ28	MD61
AJ29	GND

2.5 Alpha'al Pin List (SDR)

Pin No.	Pin Name
F9	5V
G6	5V
K5	AAG
AE1	AD_STB0
AE2	AD_STB0J
V3	AD_STB1
U1	AD_STB1J
J1	AD0
J2	AD1
G5	AD10
F1	AD11
F2	AD12
F3	AD13
E1	AD14
E2	AD15
A3	AD16
E4	AD17
D4	AD18
C4	AD19
J3	AD2
B4	AD20
A4	AD21
F5	AD22
D5	AD23
A5	AD24
F6	AD25
E6	AD26
C6	AD27
B6	AD28
A6	AD29
J4	AD3
F7	AD30
E7	AD31
H1	AD4
H2	AD5
H3	AD6
G1	AD7
G2	AD8
G4	AD9
T28	ADSJ
AA1	AGPDEVSELJ
Y1	AGPFRAMEJ
AB3	AGPGND
AE3	AGPGND
AF2	AGPGND
AJ1	AGPGND
K3	AGPGND
N3	AGPGND
R2	AGPGND
T3	AGPGND

Pin No.	Pin Name
V2	AGPGND
W3	AGPGND
AA3	AGPIRDYJ
AB1	AGPPAR
AC5	AGPREF
N6	AGPREF
AD4	AGPSENSE
AC3	AGPSERRJ
AC4	AGPSHL
AB2	AGPSTOPJ
AA2	AGPTRDYJ
AC6	AIGND
AD5	AIPOW1
AD6	AIPOW2
J6	AREQJ
L5	AVDDA
R28	BNRJ
N27	BPRIJ
P26	BREQJ0
G3	CBEJ0
D1	CBEJ1
B3	CBEJ2
B5	CBEJ3
AF25	CKE0
AF26	CKE1
AD22	CKE2
AE22	CKE3
AE21	CKE4
AF23	CKE5
AF5	CLK32KI
D16	CPURST
AD9	CSJ0
AE9	CSJ1
AE8	CSJ2
AF8	CSJ3
AE7	CSJ4
AD8	CSJ5
P25	DBSYJ
AD23	DCLK
AD24	DCLKJ
P28	DEFERJ
B1	DEVSELJ
AF15	DQM0
AJ15	DQM1
AH16	DQM2
AG17	DQM3
AH15	DQM4
AG16	DQM5
AJ16	DQM6
AH17	DQM7

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(SDR-Alpha-continued)

Pin No.	Pin Name
AH28	DQS0
AJ25	DQS1
AH21	DQS2
AF18	DQS3
AJ14	DQS4
AH11	DQS5
AJ7	DQS6
AH4	DQS7
T29	DRDYJ
AD20	DREF
AD7	DREF
AE13	DREF
AD21	DSHL
AE6	DSHL
C3	FRAMEJ
M12	G/T
M13	G/T
M14	G/T
M15	G/T
M16	G/T
N12	G/T
N13	G/T
N14	G/T
N15	G/T
N16	G/T
P11	G/T
P12	G/T
P13	G/T
P14	G/T
P15	G/T
P16	G/T
P17	G/T
P18	G/T
R11	G/T
R12	G/T
R13	G/T
R14	G/T
R15	G/T
R16	G/T
R17	G/T
R18	G/T
T11	G/T
T12	G/T
T13	G/T
T14	G/T
T15	G/T
T16	G/T
T17	G/T
T18	G/T
U12	G/T

Pin No.	Pin Name
U13	G/T
U14	G/T
U15	G/T
U16	G/T
U17	G/T
U18	G/T
V12	G/T
V13	G/T
V14	G/T
V15	G/T
V16	G/T
V17	G/T
V18	G/T
W14	G/T
W15	G/T
W16	G/T
AB6	GAD0
AH1	GAD1
AD2	GAD10
W4	GAD11
AD3	GAD12
W5	GAD13
AC1	GAD14
V5	GAD15
V4	GAD16
Y3	GAD17
U5	GAD18
W1	GAD19
AA4	GAD2
T4	GAD20
W2	GAD21
T5	GAD22
V1	GAD23
P4	GAD24
U2	GAD25
P5	GAD26
U3	GAD27
N4	GAD28
T1	GAD29
AG1	GAD3
N5	GAD30
T2	GAD31
AA5	GAD4
AG2	GAD5
AA6	GAD6
AF1	GAD7
AD1	GAD8
Y6	GAD9
Y5	GCBEJ0
AC2	GCBEJ1

Pin No.	Pin Name
Y2	GCBEJ2
R5	GCBEJ3
L6	GCLK
K1	GGNTJ
A11	GND
A13	GND
A15	GND
A17	GND
A19	GND
A21	GND
A23	GND
A25	GND
A27	GND
A29	GND
AA25	GND
AA29	GND
AB27	GND
AC25	GND
AC29	GND
AD12	GND
AD14	GND
AD27	GND
AE29	GND
AF4	GND
AG12	GND
AG15	GND
AG18	GND
AG21	GND
AG24	GND
AG27	GND
AG6	GND
AG9	GND
AJ29	GND
B10	GND
B12	GND
C11	GND
C13	GND
C16	GND
C18	GND
C20	GND
C22	GND
C24	GND
C26	GND
C29	GND
D10	GND
D12	GND
D27	GND
E11	GND
E13	GND
E17	GND

(SDR-Alpha-continued)

Pin No.	Pin Name
E19	GND
E21	GND
E23	GND
E24	GND
E25	GND
E29	GND
F10	GND
F12	GND
F16	GND
F17	GND
F24	GND
F27	GND
G25	GND
G29	GND
H27	GND
J25	GND
J29	GND
K27	GND
L24	GND
L25	GND
L29	GND
M24	GND
M27	GND
N25	GND
N29	GND
P24	GND
P27	GND
R25	GND
R29	GND
T24	GND
T27	GND
U25	GND
U29	GND
V27	GND
W25	GND
W29	GND
Y24	GND
Y27	GND
B7	GNTJ0
C8	GNTJ1
A8	GNTJ2
A9	GNTJ3
D9	GNTJ4
E8	GNTJ5
E9	GNTJ6
L3	GREQJ
Y29	HA10
W26	HA11
AB28	HA12
AA27	HA13

Pin No.	Pin Name
AA28	HA14
Y26	HA15
W24	HA16
AD29	HA17
AC28	HA18
AB29	HA19
AA26	HA20
AC27	HA21
AD28	HA22
AE28	HA23
Y25	HA24
AE27	HA25
AC26	HA26
AF28	HA27
AA24	HA28
AF29	HA29
V29	HA3
AB25	HA30
AD26	HA31
U26	HA4
U24	HA5
W27	HA6
W28	HA7
V25	HA8
Y28	HA9
V26	HADSTB0
AB26	HADSTB1
AD25	HAG
V24	HAVREF
AC24	HCLK-
AB24	HCLK+
N24	HCVREF
M29	HD0
L28	HD1
H26	HD10
H25	HD11
H28	HD12
K25	HD13
G24	HD14
G28	HD15
F26	HD16
F28	HD17
F25	HD18
G26	HD19
L27	HD2
E27	HD20
F29	HD21
E28	HD22
G27	HD23
C28	HD24

Pin No.	Pin Name
D29	HD25
B29	HD26
B27	HD27
C27	HD28
A28	HD29
J27	HD3
D26	HD30
B28	HD31
D24	HD32
D23	HD33
D22	HD34
A26	HD35
F23	HD36
B26	HD37
C25	HD38
B25	HD39
M28	HD4
D21	HD40
A24	HD41
C23	HD42
B23	HD43
B22	HD44
A22	HD45
B21	HD46
C21	HD47
B20	HD48
A20	HD49
K24	HD5
E20	HD50
C19	HD51
D20	HD52
F19	HD53
B19	HD54
B18	HD55
C17	HD56
A18	HD57
D18	HD58
B17	HD59
K28	HD6
D17	HD60
B16	HD61
E16	HD62
A16	HD63
K29	HD7
J28	HD8
H29	HD9
L26	HDBI0
D28	HDBI1
B24	HDBI2
D19	HDBI3

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(SDR-Alpha-continued)

Pin No.	Pin Name
K26	HDSTBN0
D25	HDSTBN1
E22	HDSTBN2
E18	HDSTBN3
J26	HDSTBP0
E26	HDSTBP1
F22	HDSTBP2
F18	HDSTBP3
F21	HDVREF
J24	HDVREF
F14	HIGND
D15	HIPOW1
E15	HIPOW2
P29	HITJ
N28	HITMJ
N26	HLOCKJ
V28	HREQJ0
T25	HREQJ1
T26	HREQJ2
U28	HREQJ3
U27	HREQJ4
B14	HSCRHDN
A14	HSCRHDP
E14	HSCRSBN
D14	HSCRSBP
C14	HSCRSHI
C15	HSENSEN
B15	HSENSEP
AE26	HVDDA
F20	HVREFSHL
H24	HVREFSHL
A2	IRDYJ
AD11	MA0
AE11	MA1
AD17	MA10
AD19	MA11
AE19	MA12
AE17	BA0
AE18	BA1
AE12	MA2
AE15	MA3
AF14	MA4
AE14	MA5
AF17	MA6
AD16	MA7
AE16	MA8
AD18	MA9
AE24	MAG
AG3	MD0
AJ3	MD1

Pin No.	Pin Name
AH10	MD10
AG11	MD11
AF12	MD12
AJ12	MD13
AH13	MD14
AG14	MD15
AJ17	MD16
AJ18	MD17
AH19	MD18
AG20	MD19
AJ4	MD2
AJ20	MD20
AJ21	MD21
AH22	MD22
AJ23	MD23
AG23	MD24
AH24	MD25
AG25	MD26
AJ26	MD27
AG26	MD28
AH27	MD29
AH5	MD3
AH29	MD30
AG28	MD31
AH3	MD32
AG4	MD33
AG5	MD34
AJ5	MD35
AH6	MD36
AG7	MD37
AG8	MD38
AJ8	MD39
AF6	MD4
AH9	MD40
AG10	MD41
AJ10	MD42
AJ11	MD43
AH12	MD44
AG13	MD45
AJ13	MD46
AH14	MD47
AH18	MD48
AG19	MD49
AJ6	MD5
AJ19	MD50
AH20	MD51
AF21	MD52
AG22	MD53
AJ22	MD54
AH23	MD55

Pin No.	Pin Name
AJ24	MD56
AF24	MD57
AH25	MD58
AH26	MD59
AH7	MD6
AJ27	MD60
AJ28	MD61
AF27	MD62
AG29	MD63
AH8	MD7
AF9	MD8
AJ9	MD9
AE25	MVDDA
AF20	MWEJ
T6	NC
V6	NC
U6	NC
AB4	P1A
AB5	P1A
AE4	P1A
AF3	P1A
K4	P1A
R4	P1A
U4	P1A
Y4	P1A
AD13	P1B
AE20	P1B
AE23	P1B
AF10	P1B
AF11	P1B
AF13	P1B
AF16	P1B
AF19	P1B
AF22	P1B
AF7	P1B
L11	P2A
L12	P2A
M11	P2A
M17	P2A
M18	P2A
N11	P2A
N17	P2A
N18	P2A
U11	P2A
V11	P2A
V19	P2A
W11	P2A
W12	P2A
W13	P2A
W17	P2A

(SDR-Alpha-continued)

Pin No.	Pin Name
W18	P2A
W19	P2A
D6	P3A
E5	P3A
F4	P3A
H4	P3A
P6	P3G
W6	P3G
D2	PAR
F8	PCICLK
A1	PCIGND
C5	PCIGND
E3	PCIGND
H6	PCIRSTJ
J5	PHLDAJ
H5	PHLDJ
M2	PIPEJ
C1	PLOCKJ
R26	HTRDY J
K6	RATIOJ
M1	RBFJ
C7	REQJ0
A7	REQJ1
B8	REQJ2
B9	REQJ3
C9	REQJ4
D7	REQJ5
D8	REQJ6
R27	RSJ0
M25	RSJ1
M26	RSJ2
P1	SB_STB
P2	SB_STBJ
N1	SBA0
L4	SBA1
P3	SBA2
M6	SBA3
R3	SBA4
M5	SBA5
R1	SBA6
M4	SBA7
AD10	SCASJ
D3	SERRJ
AE10	SRASJ
L1	ST0
L2	ST1
M3	ST2
C2	STOPJ
AE5	SUSPENDJ
AJ2	TESTEN1

Pin No.	Pin Name
AH2	TESTMODE
B2	TRDYJ
K2	TYPEDETJ
A10	VTT
A12	VTT
B11	VTT
B13	VTT
C10	VTT
C12	VTT
D11	VTT
D13	VTT
E10	VTT
E12	VTT
F11	VTT
F13	VTT
L13	VTT
L14	VTT
L15	VTT
L16	VTT
L17	VTT
L18	VTT
L19	VTT
M19	VTT
N19	VTT
P19	VTT
R19	VTT
T19	VTT
U19	VTT
N2	WBFJ

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2.6 Numerical Pin List (DDR)

Pin No.	Pin Name
A1	PCIGND
A2	IRDYJ
A3	AD16
A4	AD21
A5	AD24
A6	AD29
A7	REQJ1
A8	GNTJ2
A9	GNTJ3
A10	VTT
A11	GND
A12	VTT
A13	GND
A14	HSCRHDP
A15	GND
A16	HD63
A17	GND
A18	HD57
A19	GND
A20	HD49
A21	GND
A22	HD45
A23	GND
A24	HD41
A25	GND
A26	HD35
A27	GND
A28	HD29
A29	GND
B1	DEVSELJ
B2	TRDYJ
B3	CBEJ2
B4	AD20
B5	CBEJ3
B6	AD28
B7	GNTJ0
B8	REQJ2
B9	REQJ3
B10	GND
B11	VTT
B12	GND
B13	VTT
B14	HSCRHDN
B15	HSENSEP
B16	HD61
B17	HD59
B18	HD55
B19	HD54
B20	HD48
B21	HD46

Pin No.	Pin Name
B22	HD44
B23	HD43
B24	HDBI2
B25	HD39
B26	HD37
B27	HD27
B28	HD31
B29	HD26
C1	PLOCKJ
C2	STOPJ
C3	FRAMEJ
C4	AD19
C5	PCIGND
C6	AD27
C7	REQJ0
C8	GNTJ1
C9	REQJ4
C10	VTT
C11	GND
C12	VTT
C13	GND
C14	HSCRSHI
C15	HSENSEN
C16	GND
C17	HD56
C18	GND
C19	HD51
C20	GND
C21	HD47
C22	GND
C23	HD42
C24	GND
C25	HD38
C26	GND
C27	HD28
C28	HD24
C29	GND
D1	CBEJ1
D2	PAR
D3	SERRJ
D4	AD18
D5	AD23
D6	P3A
D7	REQJ5
D8	REQJ6
D9	GNTJ4
D10	GND
D11	VTT
D12	GND
D13	VTT

Pin No.	Pin Name
D14	HSCRSBP
D15	HIPOW1
D16	CPURST
D17	HD60
D18	HD58
D19	HDBI3
D20	HD52
D21	HD40
D22	HD34
D23	HD33
D24	HD32
D25	HDSTBN1
D26	HD30
D27	GND
D28	HDBI1
D29	HD25
E1	AD14
E2	AD15
E3	PCIGND
E4	AD17
E5	P3A
E6	AD26
E7	AD31
E8	GNTJ5
E9	GNTJ6
E10	VTT
E11	GND
E12	VTT
E13	GND
E14	HSCRSBN
E15	HIPOW2
E16	HD62
E17	GND
E18	HDSTBN3
E19	GND
E20	HD50
E21	GND
E22	HDSTBN2
E23	GND
E24	GND
E25	GND
E26	HDSTBP1
E27	HD20
E28	HD22
E29	GND
F1	AD11
F2	AD12
F3	AD13
F4	P3A
F5	AD22

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(continued-DDR)

Pin No.	Pin Name
F6	AD25
F7	AD30
F8	PCICLK
F9	5V
F10	GND
F11	VTT
F12	GND
F13	VTT
F14	HIGND
F16	GND
F17	GND
F18	HDSTBP3
F19	HD53
F20	HVREFSHL
F21	HDVREF
F22	HDSTBP2
F23	HD36
F24	GND
F25	HD18
F26	HD16
F27	GND
F28	HD17
F29	HD21
G1	AD7
G2	AD8
G3	CBEJ0
G4	AD9
G5	AD10
G6	5V
G24	HD14
G25	GND
G26	HD19
G27	HD23
G28	HD15
G29	GND
H1	AD4
H2	AD5
H3	AD6
H4	P3A
H5	PHLDJ
H6	PCIRSTJ
H24	HVREFSHL
H25	HD11
H26	HD10
H27	GND
H28	HD12
H29	HD9
J1	AD0
J2	AD1
J3	AD2

Pin No.	Pin Name
J4	AD3
J5	PHLDAJ
J6	AREQJ
J24	HDVREF
J25	GND
J26	HDSTBP0
J27	HD3
J28	HD8
J29	GND
K1	GGNTJ
K2	TYPEDETJ
K3	AGPGND
K4	P1A
K5	AAG
K6	RATIOJ
K24	HD5
K25	HD13
K26	HDSTBN0
K27	GND
K28	HD6
K29	HD7
L1	ST0
L2	ST1
L3	GREQJ
L4	SBA1
L5	AVDDA
L6	GCLK
L11	P2A
L12	P2A
L13	VTT
L14	VTT
L15	VTT
L16	VTT
L17	VTT
L18	VTT
L19	VTT
L24	GND
L25	GND
L26	HDBI0
L27	HD2
L28	HD1
L29	GND
M1	RBFJ
M2	PIPEJ
M3	ST2
M4	SBA7
M5	SBA5
M6	SBA3
M11	P2A
M12	G/T

Pin No.	Pin Name
M13	G/T
M14	G/T
M15	G/T
M16	G/T
M17	P2A
M18	P2A
M19	VTT
M24	GND
M25	RSJ1
M26	RSJ2
M27	GND
M28	HD4
M29	HD0
N1	SBA0
N2	WBFJ
N3	AGPGND
N4	GAD28
N5	GAD30
N6	AGPREF
N11	P2A
N12	G/T
N13	G/T
N14	G/T
N15	G/T
N16	G/T
N17	P2A
N18	P2A
N19	VTT
N24	HCVREF
N25	GND
N26	HLOCKJ
N27	BPRIJ
N28	HITMJ
N29	GND
P1	SB_STB
P2	SB_STBJ
P3	SBA2
P4	GAD24
P5	GAD26
P6	P3G
P11	G/T
P12	G/T
P13	G/T
P14	G/T
P15	G/T
P16	G/T
P17	G/T
P18	G/T
P19	VTT
P24	GND

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Pin No.	Pin Name
P25	DBSYJ
P26	BREQJ0
P27	GND
P28	DEFERJ
P29	HITJ
R1	SBA6
R2	AGPGND
R3	SBA4
R4	P1A
R5	GCBEJ3
R11	G/T
R12	G/T
R13	G/T
R14	G/T
R15	G/T
R16	G/T
R17	G/T
R18	G/T
R19	VTT
R25	GND
R26	HTRDY J
R27	RSJ0
R28	BNRJ
R29	GND
T1	GAD29
T2	GAD31
T3	AGPGND
T4	GAD20
T5	GAD22
T6	NC
T11	G/T
T12	G/T
T13	G/T
T14	G/T
T15	G/T
T16	G/T
T17	G/T
T18	G/T
T19	VTT
T24	GND
T25	HREQJ1
T26	HREQJ2
T27	GND
T28	ADSJ
T29	DRDYJ
U1	AD_STB1J
U2	GAD25
U3	GAD27
U4	P1A
U5	GAD18

Pin No.	Pin Name
U6	NC
U11	P2A
U12	G/T
U13	G/T
U14	G/T
U15	G/T
U16	G/T
U17	G/T
U18	G/T
U19	VTT
U24	HA5
U25	GND
U26	HA4
U27	HREQJ4
U28	HREQJ3
U29	GND
V1	GAD23
V2	AGPGND
V3	AD_STB1
V4	GAD16
V5	GAD15
V6	NC
V11	P2A
V12	G/T
V13	G/T
V14	G/T
V15	G/T
V16	G/T
V17	G/T
V18	G/T
V19	P2A
V24	HAVREF
V25	HA8
V26	HADSTB0
V27	GND
V28	HREQJ0
V29	HA3
W1	GAD19
W2	GAD21
W3	AGPGND
W4	GAD11
W5	GAD13
W6	P3G
W11	P2A
W12	P2A
W13	P2A
W14	G/T
W15	G/T
W16	G/T
W17	P2A

Pin No.	Pin Name
W18	P2A
W19	P2A
W24	HA16
W25	GND
W26	HA11
W27	HA6
W28	HA7
W29	GND
Y1	AGPFRAMEJ
Y2	GCBEJ2
Y3	GAD17
Y4	P1A
Y5	GCBEJ0
Y6	GAD9
Y24	GND
Y25	HA24
Y26	HA15
Y27	GND
Y28	HA9
Y29	HA10
AA1	AGPDEVSELJ
AA2	AGPTRDYJ
AA3	AGPIRDYJ
AA4	GAD2
AA5	GAD4
AA6	GAD6
AA24	HA28
AA25	GND
AA26	HA20
AA27	HA13
AA28	HA14
AA29	GND
AB1	AGPPAR
AB2	AGPSTOPJ
AB3	AGPGND
AB4	P1A
AB5	P1A
AB6	GAD0
AB24	HCLK+
AB25	HA30
AB26	HADSTB1
AB27	GND
AB28	HA12
AB29	HA19
AC1	GAD14
AC2	GCBEJ1
AC3	AGPSERRJ
AC4	AGPSHL
AC5	AGPREF
AC6	AIGND

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Pin No.	Pin Name
AC24	HCLK-
AC25	GND
AC26	HA26
AC27	HA21
AC28	HA18
AC29	GND
AD1	GAD8
AD2	GAD10
AD3	GAD12
AD4	AGPSENSE
AD5	AIPOW1
AD6	AIPOW2
AD7	DVREF
AD8	CSJ4
AD9	CSJ0
AD10	MWEJ
AD11	SRASJ
AD12	GND
AD13	P1B
AD14	GND
AD16	A3
AD17	A5
AD18	A7
AD19	A9
AD20	DVREF
AD21	DSHL
AD22	CKE5
AD23	DCLK
AD24	DCLKJ
AD25	HAG
AD26	HA31
AD27	GND
AD28	HA22
AD29	HA17
AE1	AD_STB0
AE2	AD_STB0J
AE3	AGPGND
AE4	P1A
AE5	SUSPENDJ
AE6	DSHL
AE7	CSJ5
AE8	CSJ2
AE9	CSJ1
AE10	SCASJ
AE11	ABA0
AE12	ABA1
AE13	DVREF
AE14	A0
AE15	A1
AE16	A2

Pin No.	Pin Name
AE17	A4
AE18	A8
AE19	A11
AE20	P1B
AE21	CKE4
AE22	CKE2
AE23	P1B
AE24	MAG
AE25	MVDDA
AE26	HVDDA
AE27	HA25
AE28	HA23
AE29	GND
AF1	GAD7
AF2	AGPGND
AF3	P1A
AF4	GND
AF5	CLK32KI
AF6	MD60
AF7	P1B
AF8	CSJ3
AF9	MD49
AF10	P1B
AF11	P1B
AF12	MD45
AF13	P1B
AF14	A10
AF15	MD37
AF16	P1B
AF17	A6
AF18	DQS3
AF19	P1B
AF20	A12
AF21	DM2
AF22	P1B
AF23	CKE3
AF24	MD13
AF25	CKE0
AF26	CKE1
AF27	MD5
AF28	HA27
AF29	HA29
AG1	GAD3
AG2	GAD5
AG3	MD59
AG4	MD62
AG5	MD57
AG6	GND
AG7	MD50
AG8	DM6

Pin No.	Pin Name
AG9	GND
AG10	MD46
AG11	DM5
AG12	GND
AG13	MD35
AG14	DM4
AG15	GND
AG16	MD32
AG17	MD30
AG18	GND
AG19	MD28
AG20	MD19
AG21	GND
AG22	MD17
AG23	MD15
AG24	GND
AG25	MD9
AG26	MD7
AG27	GND
AG28	MD4
AG29	MD0
AH1	GAD1
AH2	TESTMODE
AH3	MD63
AH4	DQS7
AH5	MD61
AH6	MD51
AH7	MD54
AH8	MD53
AH9	MD48
AH10	MD43
AH11	DQS5
AH12	MD44
AH13	MD39
AH14	MD34
AH15	MD33
AH16	MD31
AH17	MD26
AH18	MD29
AH19	MD24
AH20	MD22
AH21	DQS2
AH22	MD16
AH23	MD10
AH24	DM1
AH25	MD12
AH26	MD3
AH27	MD2
AH28	DQS0
AH29	MD1

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Pin No.	Pin Name
AJ1	AGPGND
AJ2	TESTEN1
AJ3	MD58
AJ4	DM7
AJ5	MD56
AJ6	MD55
AJ7	DQS6
AJ8	MD52
AJ9	MD47
AJ10	MD42
AJ11	MD41
AJ12	MD40
AJ13	MD38
AJ14	DQS4
AJ15	MD36
AJ16	MD27
AJ17	DM3
AJ18	MD25
AJ19	MD23
AJ20	MD18
AJ21	MD21
AJ22	MD20
AJ23	MD11
AJ24	MD14
AJ25	DQS1
AJ26	MD8
AJ27	MD6
AJ28	DM0
AJ29	GND

Pin No.	Pin Name
F9	5V
G6	5V
AE14	A0
AE15	A1
AF14	A10
AE19	A11
AF20	A12
AE16	A2
AD16	A3
AE17	A4
AD17	A5
AF17	A6
AD18	A7
AE18	A8
AD19	A9
K5	AAG
AE1	AD_STB0
AE2	AD_STB0J
V3	AD_STB1
U1	AD_STB1J
J1	AD0
J2	AD1
G5	AD10
F1	AD11
F2	AD12
F3	AD13
E1	AD14
E2	AD15
A3	AD16
E4	AD17
D4	AD18
C4	AD19
J3	AD2
B4	AD20
A4	AD21
F5	AD22
D5	AD23
A5	AD24
F6	AD25
E6	AD26
C6	AD27
B6	AD28
A6	AD29
J4	AD3
F7	AD30
E7	AD31
H1	AD4
H2	AD5
H3	AD6
G1	AD7

Pin No.	Pin Name
G2	AD8
G4	AD9
T28	ADSJ
AA1	AGPDEVSELJ
Y1	AGPFRAMEJ
AB3	AGPGND
AE3	AGPGND
AF2	AGPGND
AJ1	AGPGND
K3	AGPGND
N3	AGPGND
R2	AGPGND
T3	AGPGND
V2	AGPGND
W3	AGPGND
AA3	AGPIRDYJ
AB1	AGPPAR
AC5	AGPREF
N6	AGPREF
AD4	AGPSENSE
AC3	AGPSERRJ
AC4	AGPSHL
AB2	AGPSTOPJ
AA2	AGPTRDYJ
AC6	AIGND
AD5	AIPOW1
AD6	AIPOW2
J6	AREQJ
L5	AVDDA
AE11	BA0
AE12	BA1
R28	BNRJ
N27	BPRIJ
P26	BREQJ0
G3	CBEJ0
D1	CBEJ1
B3	CBEJ2
B5	CBEJ3
AF25	CKE0
AF26	CKE1
AE22	CKE2
AF23	CKE3
AE21	CKE4
AD22	CKE5
AF5	CLK32KI
D16	CPURST
AD9	CSJ0
AE9	CSJ1
AE8	CSJ2
AF8	CSJ3

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Pin No.	Pin Name
AD8	CSJ4
AE7	CSJ5
P25	DBSYJ
AD23	DCLK
AD24	DCLKJ
P28	DEFERJ
B1	DEVSELJ
AJ28	DM0
AH24	DM1
AF21	DM2
AJ17	DM3
AG14	DM4
AG11	DM5
AG8	DM6
AJ4	DM7
AH28	DQS0
AJ25	DQS1
AH21	DQS2
AF18	DQS3
AJ14	DQS4
AH11	DQS5
AJ7	DQS6
AH4	DQS7
T29	DRDYJ
AD21	DSHL
AE6	DSHL
AD20	DVREF
AD7	DVREF
AE13	DVREF
C3	FRAMEJ
M12	G/T
M13	G/T
M14	G/T
M15	G/T
M16	G/T
N12	G/T
N13	G/T
N14	G/T
N15	G/T
N16	G/T
P11	G/T
P12	G/T
P13	G/T
P14	G/T
P15	G/T
P16	G/T
P17	G/T
P18	G/T
R11	G/T
R12	G/T

Pin No.	Pin Name
R13	G/T
R14	G/T
R15	G/T
R16	G/T
R17	G/T
R18	G/T
T11	G/T
T12	G/T
T13	G/T
T14	G/T
T15	G/T
T16	G/T
T17	G/T
T18	G/T
U12	G/T
U13	G/T
U14	G/T
U15	G/T
U16	G/T
U17	G/T
U18	G/T
V12	G/T
V13	G/T
V14	G/T
V15	G/T
V16	G/T
V17	G/T
V18	G/T
W14	G/T
W15	G/T
W16	G/T
AB6	GAD0
AH1	GAD1
AD2	GAD10
W4	GAD11
AD3	GAD12
W5	GAD13
AC1	GAD14
V5	GAD15
V4	GAD16
Y3	GAD17
U5	GAD18
W1	GAD19
AA4	GAD2
T4	GAD20
W2	GAD21
T5	GAD22
V1	GAD23
P4	GAD24
U2	GAD25

Pin No.	Pin Name
P5	GAD26
U3	GAD27
N4	GAD28
T1	GAD29
AG1	GAD3
N5	GAD30
T2	GAD31
AA5	GAD4
AG2	GAD5
AA6	GAD6
AF1	GAD7
AD1	GAD8
Y6	GAD9
Y5	GCBEJ0
AC2	GCBEJ1
Y2	GCBEJ2
R5	GCBEJ3
L6	GCLK
K1	GGNTJ
A11	GND
A13	GND
A15	GND
A17	GND
A19	GND
A21	GND
A23	GND
A25	GND
A27	GND
A29	GND
AA25	GND
AA29	GND
AB27	GND
AC25	GND
AC29	GND
AD12	GND
AD14	GND
AD27	GND
AE29	GND
AF4	GND
AG12	GND
AG15	GND
AG18	GND
AG21	GND
AG24	GND
AG27	GND
AG6	GND
AG9	GND
AJ29	GND
B10	GND
B12	GND

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Pin No.	Pin Name
C11	GND
C13	GND
C16	GND
C18	GND
C20	GND
C22	GND
C24	GND
C26	GND
C29	GND
D10	GND
D12	GND
D27	GND
E11	GND
E13	GND
E17	GND
E19	GND
E21	GND
E23	GND
E24	GND
E25	GND
E29	GND
F10	GND
F12	GND
F16	GND
F17	GND
F24	GND
F27	GND
G25	GND
G29	GND
H27	GND
J25	GND
J29	GND
K27	GND
L24	GND
L25	GND
L29	GND
M24	GND
M27	GND
N25	GND
N29	GND
P24	GND
P27	GND
R25	GND
R29	GND
T24	GND
T27	GND
U25	GND
U29	GND
V27	GND
W25	GND

Pin No.	Pin Name
W29	GND
Y24	GND
Y27	GND
B7	GNTJ0
C8	GNTJ1
A8	GNTJ2
A9	GNTJ3
D9	GNTJ4
E8	GNTJ5
E9	GNTJ6
L3	GREQJ
Y29	HA10
W26	HA11
AB28	HA12
AA27	HA13
AA28	HA14
Y26	HA15
W24	HA16
AD29	HA17
AC28	HA18
AB29	HA19
AA26	HA20
AC27	HA21
AD28	HA22
AE28	HA23
Y25	HA24
AE27	HA25
AC26	HA26
AF28	HA27
AA24	HA28
AF29	HA29
V29	HA3
AB25	HA30
AD26	HA31
U26	HA4
U24	HA5
W27	HA6
W28	HA7
V25	HA8
Y28	HA9
V26	HADSTB0
AB26	HADSTB1
AD25	HAG
V24	HAVREF
AC24	HCLK-
AB24	HCLK+
N24	HCVREF
M29	HD0
L28	HD1
H26	HD10

Pin No.	Pin Name
H25	HD11
H28	HD12
K25	HD13
G24	HD14
G28	HD15
F26	HD16
F28	HD17
F25	HD18
G26	HD19
L27	HD2
E27	HD20
F29	HD21
E28	HD22
G27	HD23
C28	HD24
D29	HD25
B29	HD26
B27	HD27
C27	HD28
A28	HD29
J27	HD3
D26	HD30
B28	HD31
D24	HD32
D23	HD33
D22	HD34
A26	HD35
F23	HD36
B26	HD37
C25	HD38
B25	HD39
M28	HD4
D21	HD40
A24	HD41
C23	HD42
B23	HD43
B22	HD44
A22	HD45
B21	HD46
C21	HD47
B20	HD48
A20	HD49
K24	HD5
E20	HD50
C19	HD51
D20	HD52
F19	HD53
B19	HD54
B18	HD55
C17	HD56

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Pin No.	Pin Name
A18	HD57
D18	HD58
B17	HD59
K28	HD6
D17	HD60
B16	HD61
E16	HD62
A16	HD63
K29	HD7
J28	HD8
H29	HD9
L26	HDBI0
D28	HDBI1
B24	HDBI2
D19	HDBI3
K26	HDSTBN0
D25	HDSTBN1
E22	HDSTBN2
E18	HDSTBN3
J26	HDSTBP0
E26	HDSTBP1
F22	HDSTBP2
F18	HDSTBP3
F21	HDVREF
J24	HDVREF
F14	HIGND
D15	HIPOW1
E15	HIPOW2
P29	HITJ
N28	HITMJ
N26	HLOCKJ
V28	HREQJ0
T25	HREQJ1
T26	HREQJ2
U28	HREQJ3
U27	HREQJ4
B14	HSCRHDN
A14	HSCRHDP
E14	HSCRSBN
D14	HSCRSBP
C14	HSCRSHI
C15	HSENSEN
B15	HSENSEP
R26	HTRDY J
AE26	HVDDA
F20	HVREFSHL
H24	HVREFSHL
A2	IRDYJ
AE24	MAG
AG29	MD0

Pin No.	Pin Name
AH29	MD1
AH23	MD10
AJ23	MD11
AH25	MD12
AF24	MD13
AJ24	MD14
AG23	MD15
AH22	MD16
AG22	MD17
AJ20	MD18
AG20	MD19
AH27	MD2
AJ22	MD20
AJ21	MD21
AH20	MD22
AJ19	MD23
AH19	MD24
AJ18	MD25
AH17	MD26
AJ16	MD27
AG19	MD28
AH18	MD29
AH26	MD3
AG17	MD30
AH16	MD31
AG16	MD32
AH15	MD33
AH14	MD34
AG13	MD35
AJ15	MD36
AF15	MD37
AJ13	MD38
AH13	MD39
AG28	MD4
AJ12	MD40
AJ11	MD41
AJ10	MD42
AH10	MD43
AH12	MD44
AF12	MD45
AG10	MD46
AJ9	MD47
AH9	MD48
AF9	MD49
AF27	MD5
AG7	MD50
AH6	MD51
AJ8	MD52
AH8	MD53
AH7	MD54

Pin No.	Pin Name
AJ6	MD55
AJ5	MD56
AG5	MD57
AJ3	MD58
AG3	MD59
AJ27	MD6
AF6	MD60
AH5	MD61
AG4	MD62
AH3	MD63
AG26	MD7
AJ26	MD8
AG25	MD9
AE25	MVDDA
AD10	MWEJ
T6	NC
V6	NC
U6	NC
AB4	P1A
AB5	P1A
AE4	P1A
AF3	P1A
K4	P1A
R4	P1A
U4	P1A
Y4	P1A
AD13	P1B
AE20	P1B
AE23	P1B
AF10	P1B
AF11	P1B
AF13	P1B
AF16	P1B
AF19	P1B
AF22	P1B
AF7	P1B
L11	P2A
L12	P2A
M11	P2A
M17	P2A
M18	P2A
N11	P2A
N17	P2A
N18	P2A
U11	P2A
V11	P2A
V19	P2A
W11	P2A
W12	P2A
W13	P2A

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Pin No.	Pin Name
W17	P2A
W18	P2A
W19	P2A
D6	P3A
E5	P3A
F4	P3A
H4	P3A
P6	P3G
W6	P3G
D2	PAR
F8	PCICLK
A1	PCIGND
C5	PCIGND
E3	PCIGND
H6	PCIRSTJ
J5	PHLDAJ
H5	PHLDJ
M2	PIPEJ
C1	PLOCKJ
K6	RATIOJ
M1	RBFJ
C7	REQJ0
A7	REQJ1
B8	REQJ2
B9	REQJ3
C9	REQJ4
D7	REQJ5
D8	REQJ6
R27	RSJ0
M25	RSJ1
M26	RSJ2
P1	SB_STB
P2	SB_STBJ
N1	SBA0
L4	SBA1
P3	SBA2
M6	SBA3
R3	SBA4
M5	SBA5
R1	SBA6
M4	SBA7
AE10	SCASJ
D3	SERRJ
AD11	SRASJ
L1	ST0
L2	ST1
M3	ST2
C2	STOPJ
AE5	SUSPENDJ
AJ2	TESTEN1

Pin No.	Pin Name
AH2	TESTMODE
B2	TRDYJ
K2	TYPEDETJ
A10	VTT
A12	VTT
B11	VTT
B13	VTT
C10	VTT
C12	VTT
D11	VTT
D13	VTT
E10	VTT
E12	VTT
F11	VTT
F13	VTT
L13	VTT
L14	VTT
L15	VTT
L16	VTT
L17	VTT
L18	VTT
L19	VTT
M19	VTT
N19	VTT
P19	VTT
R19	VTT
T19	VTT
U19	VTT
N2	WBFJ

2.8 Hardware Setup Table

Pin Name	Function	Register Index	Reserve pull-low resistor layout	Require Pull-low resistor (2.2 Kohm)	Reserve pull-high resistor layout	Require Pull-high resistor (10 Kohm)
ST[2]	**PLL_EN, internal PLL enable/disable** Pull-high: Enable (for normal function) Pull-low: Disable	0xDC(7)/ 0xDD(7)/ 0xDE(7)	No	----	Yes	Yes
ST[1]	**IntPLLSel(5)**, select number of stages of PLL compensation Reference Configuration Registers.	0xDC(5)/ 0xDD(5)/ 0xDE(5)	Yes	Yes	Yes	No
ST[0]	**IntPLLSel(4)**, select number of stages of PLL compensation Reference Configuration Registers.	0xDC(4) / 0xDD(4)/ 0xDE(4)	Yes	Yes	Yes	No
CBE[3]#	**IntPLLSel(3)**, select number of stages of PLL compensation Reference Configuration Registers.	0xDC(3) / 0xDD(3)/ 0xDE(3)	Yes	Yes	Yes	No
CBE[2]#	**IntPLLSel(2)**, select number of stages of PLL compensation Reference Configuration Registers.	0xDC(2) / 0xDD(2)/ 0xDE(2)	Yes	No	Yes	Yes
CBE[1]#	**IntPLLSel(1)**, select number of stages of PLL compensation Reference Configuration Registers.	0xDC(1) / 0xDD(1)/ 0xDE(1)	Yes	Yes	Yes	No
CBE[0]#	**IntPLLSel(0)**, select number of stages of PLL compensation Reference Configuration Registers.	0xDC(0) / 0xDD(0)/ 0xDE(0)	Yes	Yes	Yes	No
AREQ#	**Reserved**, must be pulled high.		No	----	Yes	Yes
SERR#	**Reserved** Pull-high: Normal mode Pull-low: Test mode		No	----	Yes	Yes
GGNT#	**Reserved**, for internal PLL test mode Pull-high: Disable PLL test mode Pull-low: Enable PLL test mode		No	----	Yes	Yes
AD[10:0]	**Reserved**		No	----	No	----
AD[11]	**CPU Bus Driving Control Mode** Pull-high: By Tracking Circuit Pull-low: By AD[17:12] hardware setting		Yes	No	Yes	Yes
AD[14:12]	**CPU Bus Termination Strength Control** (when AD[11] is pulled low) 000: Default Termination 001: Default + 1X Termination 010: Default + 2X Termination ..... 111: Default + 7X Termination Pull-high: Logic 1 Pull-low: Logic 0		Yes	AD[14] : No AD[13] : Yes AD[12] : Yes	Yes	AD[14] : Yes AD[13] : No AD[12] : No
AD[17:15]	**CPU Bus Driving Low Strength Control** (when AD[11] is pulled low) 000: Default Driving 001: Default + 1X Driving 010: Default + 2X Driving ..... 111: Default + 7X Driving Pull-high: Logic 1 Pull-low: Logic 0		Yes	AD[17] : No AD[16] : Yes AD[15] : Yes	Yes	AD[17] : Yes AD[16] : No AD[15] : No

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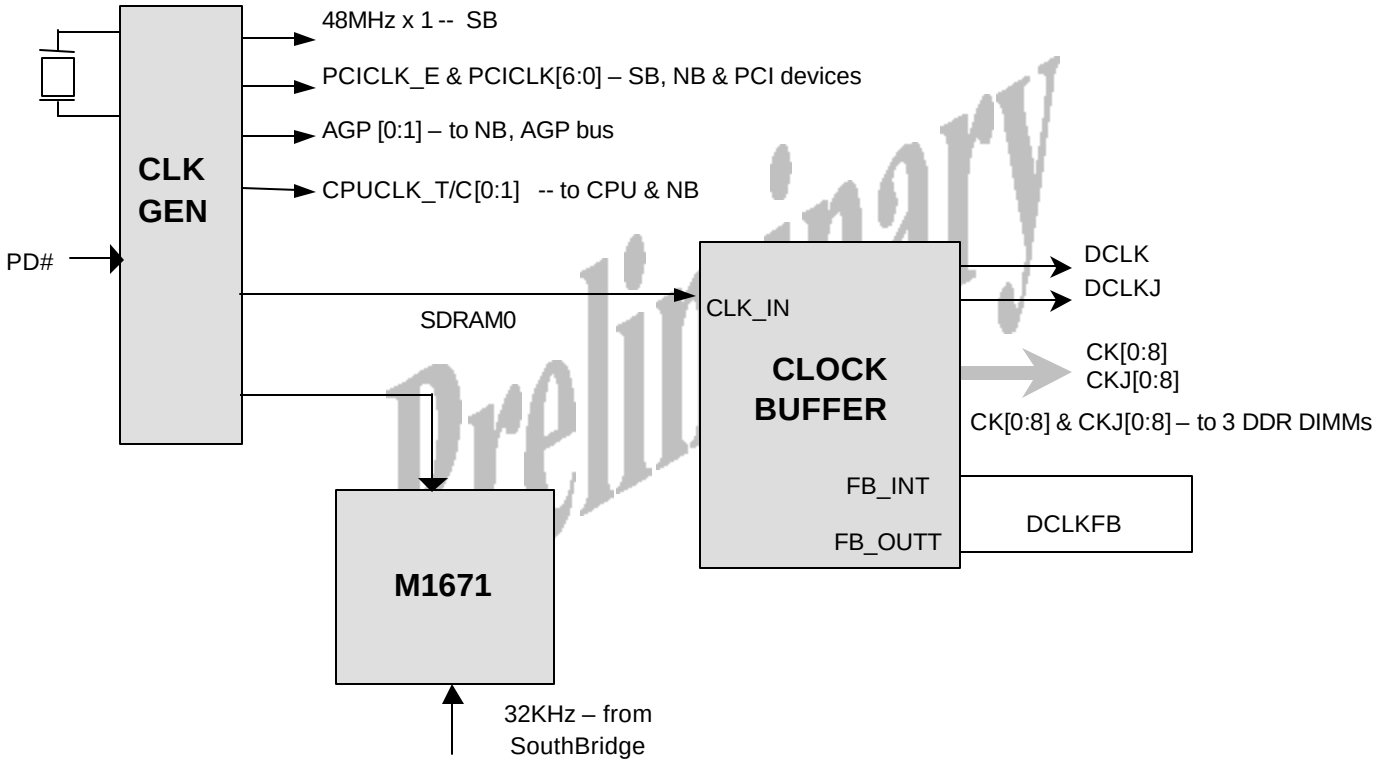
(Continued)

Pin Name	Function		Reserve pull-low resistor layout	Require Pull-low resistor (2.2 Kohm)	Reserve pull-high resistor layout	Require Pull-high resistor (10 Kohm)
AD[18]	**DRAM Type Selection** Pull-high: DDR Pull-low: SDR		Yes	DDR : No SDR : Yes	Yes	DDR : Yes SDR : No
AD[19]	**CPU Bus Strobe Timing Control** Pull-high: Multiply Mode Pull-low: Offset Mode		Yes	No	Yes	Yes
AD[23:20]	**CPU Address/Command Bus Strobe** *Timing Control Offset mode*: 0000: 1-stage delay (~150ps) 0001: 2-stage delay ..... 1111: 16-stage delay *Multiply mode*: 0000: 1/32 front-side bus cycle time 0001: 2/32 front-side bus cycle time .... 1111: 16/32 front-side bus cycle time Pull-high: Logic 1 Pull-low: Logic 0		Yes	AD[23] : No AD[22] :Yes AD[21] : Yes AD[20] : Yes	Yes	AD[23] : Yes AD[22] : No AD[21] : No AD[20] : No
AD[27:24]	**CPU Data Bus Strobe (N) Timing Control** *Offset mode*: 0000: 1-stage delay (~150ps) 0001: 2-stage delay ..... 1111: 16-stage delay *Multiply mode*: 0000: 1/64 front-side bus cycle time 0001: 2/64 front-side bus cycle time .... 1111: 16/64 front-side bus cycle time Pull-high: Logic 1 Pull-low: Logic 0		Yes	AD[27] : Yes AD[26] : No AD[25] : No AD[24] : Yes	Yes	AD[27] : No AD[26] : Yes AD[25] : Yes AD[24] : No
AD[31:28]	**CPU Data Bus Strobe (P) Timing Control** *Offset mode*: 0000: 1-stage delay (~ 150ps) 0001: 2-stage delay ..... 1111: 16-stage delay *Multiply mode*: 0000: 1/64 front-side bus cycle time 0001: 2/64 front-side bus cycle time .... 1111: 16/64 front-side bus cycle time Pull-high: Logic 1 Pull-low: Logic 0		Yes	AD[31] : Yes AD[30] : No AD[29] : No AD[28] : Yes	Yes	AD[31] : No AD[30] : Yes AD[29] : Yes AD[28] : No

Section 3 Function Description

3.1 M1671 System Clock Structure (DDR)

CPU clock up to 100MHz and 3 DDR DIMMs slot solution



The M1671 is designed with the following clock sources to perform the north-bridge functions:

HCLK+/HCLK- CPUCLKT[1] and CPUCLKC[1] from the clock generator; clock source for the CPU interface. This clock must be synchronous with the differential clock pair CPUCLKT[0] & CPUCLKC[0] that are clock sources for the CPU. The skew between the M1671 and CPU must be kept low.

DCLK+/DCLK- This clock pair from the clock buffer, clock source for the memory interface. This clock must be synchronous with the differential pairs CK[0:8] & CKJ[0:8] which are the clock sources for the DIMMs. The skew between the M1671 and DRAM devices on DIMM modules must be kept low, on the other hand, keep both CPUCLKT[0:1] and DCLK+/DCLK- in-phase. By clock generator specifications, the skew between HCLK+ and SDRAM0 should be programmable.

GCLKI AGP[0] from clock generator, clock source for AGP interface. This clock must synchronize with the clock AGP[1] which is clock source of AGP add-on card on AGP slot, and keep low skew between M1671 and AGP device on the AGP add-on card. On the other hand, GCLKI must lag to HCLK, DCLK+/DCLK- for 1ns~3ns for M1671 handling phase relationship between different clock source domains.

PCICLK PCICLK from clock generator, clock source for M1671 PCI interface. This clock is designed synchronously with CPUCLKT[0:1], the skew can be programmable on clock generator. However, PCI[6:0] which are clock source of PCI devices, and keep low skew between M1671 and PCI devices on the PCI add-on cards. On the other hand, PCICLK must lag to HCLK, DCLK+/DCLK- for 1ns~3ns for M1671 handling phase relationship between different clock source domains.

CLK32KI CLK32KO from ALi south-bridge, clock source for DRAM refresh at standby, S1 and S3 state.

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The clock generator on M1671 clock system also defines below functions to fulfill system power management requirements.

CPU_STOP# CPU_STOP# from ALi south-bridge. The output clocks of CPU DRAM and AGP will be gated off and keep low when CPU_STOP# is asserted. Notice that for ALi chipset clock system definition, the stop CPU clock come with stop DRAM and AGP clocks, such that system can gain further power saving since DRAM and AGP subsystem do not need to operate at this state.

PCI_STOP# PCI_STOP# from ALi south-bridge. The output clocks of PCI, will be gated off and keep low when PCI_STOP# asserted. One of the major causes to enter this mode comes from the CLKRUN# signaling which is derived from PCI mobile standard specification.

PD# Power down control pin of clock generator. All output clocks of clock generator will be stopped due to internal oscillation stop when PD# is asserted. Compare with CPU_STOP# and PCI_STOP#, the system is put into a deeper green mode at this state. The recovery time of this mode requires longer than CPU_STOP# and PCI_STOP# mode since the clock chip's settling time of oscillation circuitry and lock time of phase lock loop need longer time.

3.2 M1671 Power Plane Design Philosophy

The M1671 requires four input supply voltages: VTT, 2.5V, 3.3V and 5.0V. Connect the P2A, HVDDA, MVDDA, AVDDA, HIPOW2, AIPOW2 pins to a 2.5V power supply. These pins supply all the core voltage for the chip, the internal PLL and the I/O impedance matching circuitry. Connect the 3.3V supply to the P3A, P3G pins. 3.3V power the PCI interface and the I/O pre-driver circuitry. For a 5V PCI environment, PCI_5V must be connected to a 5V supply to provide 5V tolerance for the PCI I/O cells. To support CPU I/O Bus (GTL+) use CPU Vcore power supply on VTT pins. Pins HIPOW1, AIPOW1 are connected to CPU Vcore power source for the I/O impedance matching circuitry requirement. P1A must be connected either to 1.5V or 3.3V even if an AGP 4X adapter card is not present. Similarly, P1B must be connected to either 2.5V or 3.3V based on the presence of DDR or SDRAM memory, respectively.

3.3 M1671 Power Management Design Philosophy

The M1671 is designed not to have the chip internal power planes separated. This is a major difference between ALi previous generation ALi north-bridge chips. Analysis shows that the power consumption of a north-bridge chip itself is not a significant portion of the system power consumption if the initial design takes care of critical design issues properly. For example, using aggressive internal power down modes to minimize internal power consumption of the SRAM, PLL and I/O pad, etc. will reduce most of the power consumption of the high-speed circuitry. Individually dynamically stopping internal clocks for each functional block is another critical issue, since the chip was built using a CMOS process and will have very low current leakage when no transitions are occurring.

Therefore, for optimal system operation, all M1671 power pins need to be present during ACPI states S0, S1 and S3.

There are some power sources that the M1671 tightly couple with other parts of the system from an application point of view. Some exceptions are allowed. They are,

VTT, the GTL+ bus termination power should shut off while in the ACPI state S3.
P1A, the AGP power shared with the AGP device, should shut off while in the ACPI state S3 desktop applications.

The impedance matching circuitry powers, HIPOW1(CPU Vcore) and AIPOW1(1.5V/3.3V), are shared with VTT and P1A, respectively. They are also shut off accordingly while in the above states.
Since HVREF and AGPVREF are derived from the GTL+ bus termination power and AGP power, respectively, on system applications, they are also shut off while in the above states.

3.4 System Memory Features Description and Configuration

3.4.1 Memory Address Types Supported

The address lines are permuted as shown in the MA mapping table below to allow the M1671 to work with any available symmetric or asymmetric DRAM on the market. The M1671 DRAM sizing procedure is as follows: After determining if the DRAM is DDR or SDRAM, the BIOS then detect the column address range. Then the BIOS can select the appropriate MA mapping. (All DRAMs that have the same number of CAS address lines use the same MA mapping). After this, the BIOS then detect the row address range and calculate the DRAM size from the number of CAS and RAS address lines. The arrangement of MA mapping shown below also supports both 2-bank and 4-bank SDRAM configurations.

MA Mapping Table (64 bit DRAM)

For SDRAM (4 banks)										
64 bits	8-bit column address		9-bit column address		10-bit column address		11-bit column address		12-bit column address	
	Row address	Column address	Row address	Column address	Row address	Column address	Row address	Column address	Row address	Column address
BA1	A14	A14	A14	A14	A14	A14	A14	A14	A14	A14
BA0	A13	A13	A13	A13	A13	A13	A13	A13	A13	A13
MA12	A25		A26		A27		A28		A29	A16
MA11	A24		A25		A26		A27	A15	A28	A15
MA10	A17	P	A17	P	A17	P	A17	P	A17	P
MA9	A16		A16		A16	A12	A16	A12	A27	A12
MA8	A15		A15	A11	A15	A11	A26	A11	A26	A11
MA7	A12	A10	A12	A10	A25	A10	A25	A10	A25	A10
MA6	A11	A9	A24	A9	A24	A9	A24	A9	A24	A9
MA5	A23	A8	A23	A8	A23	A8	A23	A8	A23	A8
MA4	A22	A7	A22	A7	A22	A7	A22	A7	A22	A7
MA3	A21	A6	A21	A6	A21	A6	A21	A6	A21	A6
MA2	A20	A5	A20	A5	A20	A5	A20	A5	A20	A5
MA1	A19	A4	A19	A4	A19	A4	A19	A4	A19	A4
MA0	A18	A3	A18	A3	A18	A3	A18	A3	A18	A3

For SDRAM (2 banks)								
64 bits	8-bit column address		9-bit column address		10-bit column address		11-bit column address	
	Row address	Column address	Row address	Column address	Row address	Column address	Row address	Column address
BA0	A13	A13	A13	A13	A13	A13	A13	A13
MA12	A24		A25		A26		A27	
MA11	A23		A24		A25		A26	A15
MA10	A17	P	A17	P	A17	P	A17	P
MA9	A16		A16		A16	A12	A16	A12
MA8	A14		A14	A11	A14	A11	A14	A11
MA7	A15	A10	A15	A10	A15	A10	A25	A10
MA6	A12	A9	A12	A9	A24	A9	A24	A9
MA5	A11	A8	A23	A8	A23	A8	A23	A8
MA4	A22	A7	A22	A7	A22	A7	A22	A7
MA3	A21	A6	A21	A6	A21	A6	A21	A6
MA2	A20	A5	A20	A5	A20	A5	A20	A5
MA1	A19	A4	A19	A4	A19	A4	A19	A4
MA0	A18	A3	A18	A3	A18	A3	A18	A3

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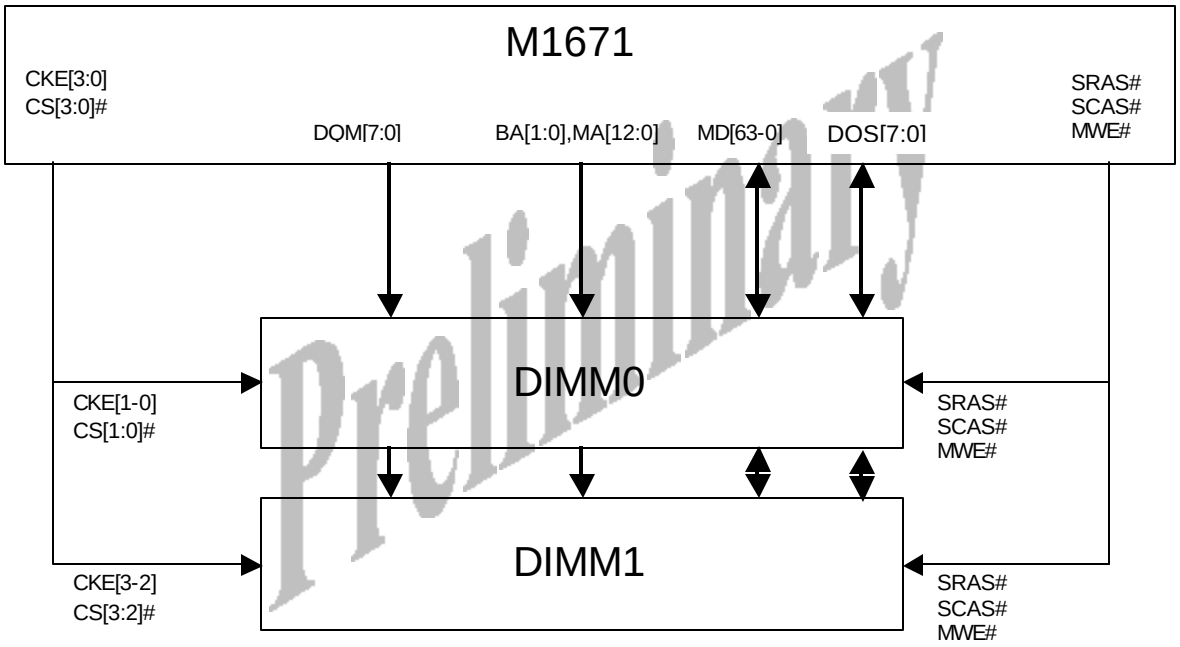
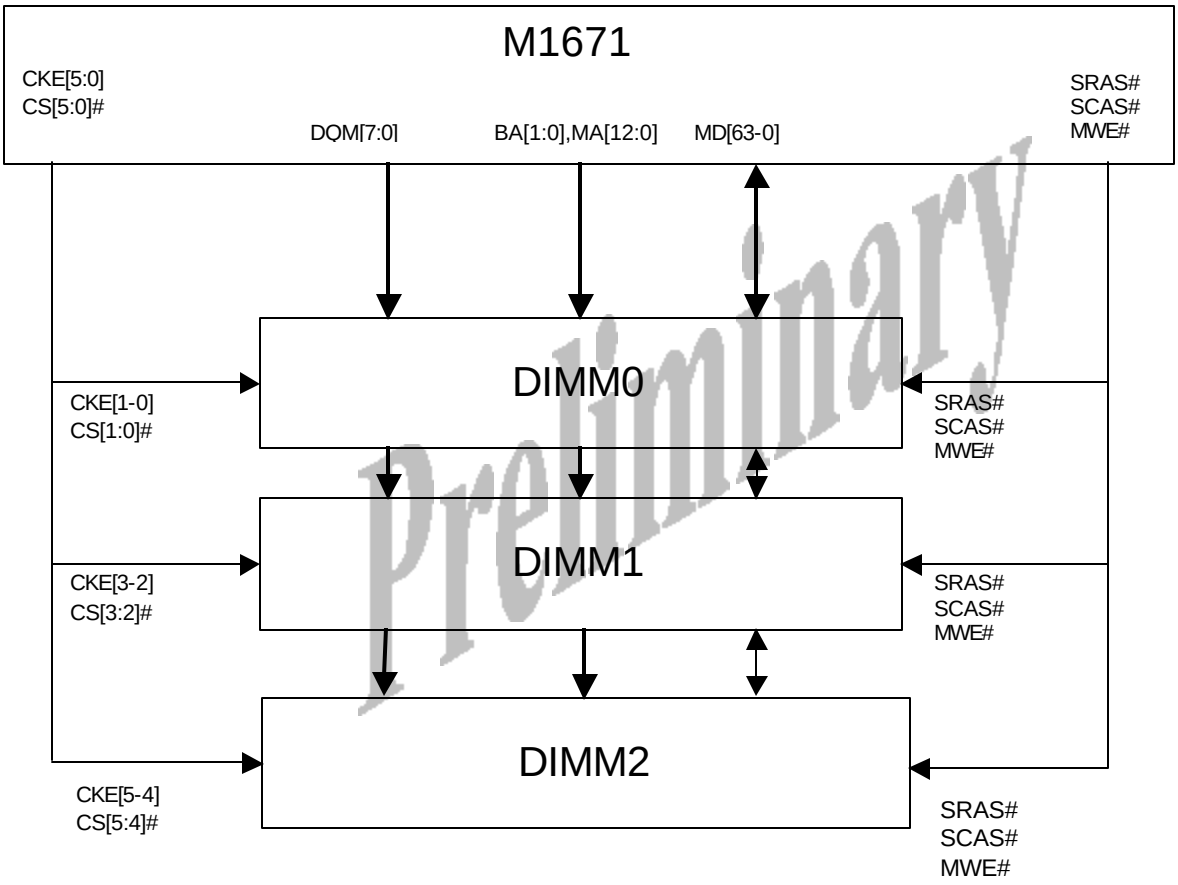
3.5 DRAM Performance Summary

DRAM performance plays a key role of system performance. M1671 has optimized the DRAM read/write operation for both latency and throughput.

3.5.1 Connection between 184-pin DDR DIMM and the M1671 in 2 DIMMs



3.5.2 Connection between 168-pin SDR DIMM and the M1671 in 3 DIMMs



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Section 4 : Configuration Registers

The following notation is used to describe the attribute of accessing registers:

RO **Read Only.** Writes to this register have no effect.
WO **Write Only.** Reading this register will return an undetermined value.
R/W **Read/Write.** A register can be read and written.
R/W Clear **Read/Write '1' Clear.** A register can be read and written, however writing a '1' will clear the corresponding bit and writing a '0' has no effect.
R/W Lock **Read, Write Lock.** A register can be read and written, however another control bit can lock the register as read only and writes to it have no effect.

M1671 PCI Mechanism #1 Configuration Register

Offset CFBh-CF8h:

Bit	Description
31	PCI Configuration ENABLE
30:24	Reserve
23:16	Bus Number
15:11	Device Number
10:8	Function Number
7:2	Register Number
1:0	Reserve

Note: The registers are accessed only when referenced as a DoubleWord.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Index	Name	Attribute	Def.value
00h-01h	Vender Identification Register	RO	10B9h
02h-03h	Device Identification Register	R/W Lock	1671h
04h-05h	Command Register	R/W	0000h
06h-07h	Status Register	R/W	0210h
08h	Revision Identification Register	R/W Lock	00h
09h	Specific Register-Level Programming Register	RO	00h
0Ah	Sub-Class Code Register	RO	00h
0Bh	Base Class Code Identification Register	RO	06h
0Ch	Cache Line Size	RO	00h
0Dh	Latency Timer	R	00h
0Eh	Header Type	R	00h
0Fh	BIST (built in self test)	R	00h
10h-13h	Base Address Register	R/W	00000008h
14h-17h	Base Address Register	R	00000000h
18h-1Bh	Base Address Register	R	00000000h
1Ch-20h	Base Address Register	R	00000000h
20h-23h	Base Address Register	R	00000000h
24h-27h	Base Address Register	R	00000000h
28h-2Bh	CardBus CIS Pointer	R	00000000h
2Ch-2Dh	Subsystem Vendor ID	R/W Lock	0000h
2Eh-2Fh	Subsystem ID	R/W Lock	0000h
30h-33h	Expansion ROM Base Address	R	00000000h
34h	Capabilities Pointer Register	R/W Lock	B0h
Control Registers for Primary PCI Bus			
40h	Control Register of PCI bridge Execution mode	R/W	1Dh
41h	Stall Retry Counter	R/W	2Fh
42h	Control Register for Posted Write/Merge of Primary PCI bridge	R/W	0Dh
43h	Special Cycle	R/W	80h
44h	Control Register 1 for PCI Master Read/Write Interface Functional Block	R/W	0Ah
45h	Control Register 2 of PCI Slave function	R/W	10h
46h	Counter for Primary PCI Delay Transaction	R/W	04h

(continued)

47h	PCI Bridge Retry Counter Register	R/W	0Ah
48h	PCI Bridge Error Command Register	R/W-One-Clear	00h
49h	PCI Bridge Error Status Register	R	00h
4Ah	Control Register of Primary PCI master functional block	R/W	00h
4Bh	PCI Arbiter Control Register	R/W	00h
4Ch	Primary PCI bus Arbiter Control Register	R/W	00h
4Dh	PCI Master Device Multiple Transaction Time Slice	R/W	20h
4Eh	PCI Bridge Multiple Transaction Time Slice	R/W	20h
4Fh-51h	Reserve	-	00h
Control Registers for Secondary PCI bus			
50h	Control Register of Secondary PCI bridge execution mode	R/W	01h
51h	Reserve	R/W	00h
52h	PCI Gated Clock Control Registers	R/W	00h
53h	Reserve	R/W	00h
54h	Control Register I for Secondary PCI Master Interface	R/W	3Bh
55h	Control Register II for Secondary PCI Master Interface	R/W	10h
56h	Expire Counter for Secondary PCI Bus Delay Transactions	R/W	04h
57h	PCI Bridge Retry Counter Register	R/W	0Ah
58h	PCI Bridge Error Command Register	R/W One Clear	00h
59h	Secondary PCI Bridge Error Status Register	R	Undefined
5Ah	Control Register of Secondary PCI Bridge	R/W	00
5Bh-5Ch	Reserve	R/W	
5Dh	Secondary PCI Master Device Multiple Transaction Time Slice	R/W	20h
5Eh	Secondary PCI Bridge Multiple Transaction Time Slice	R/W	20h
5Fh	DXI/DXO Multiple Transaction Time Slice	R/W	FFh
CPU Configuration Registers			
60h	P4 Write Order Control	R, R/W	00h
61h	Reserve	R/W	
62h	Host IO pad Driving Capability Status Register	R, R/W	
63h	Host IO Driving Capability Control Register	RO	00h
64h-69h	Host to memory frequency interface latch control function	R/W	
6Ah-6Fh	Memory to host frequency interface latch Control function	RO	00h
Memory BIU Configuration Registers:			
71h-70h 73h-72h 75h-74h	DIMM memory module/device specific parameters. 2 bytes for each DIMM module.	R/W	
76h	DRAM DIMM type/Gated Clock Global Configuration	R/W	00h
77h	DRAM Advanced Power-Saving Mode Control Register	R/W	00h
78h	MBIU GLOBAL CONFIGURATION	R/W	00h
79h	MBIU/Data Path GLOBAL Setting	R/W	10h
7Ah	DRAM Basic Timing Control Register	R/W	00h
7Bh	Miscellaneous/Paging Control	R/W	00h
7Ch-7Dh	MBIU Refresh Control Register	R/W	0000h
7Eh	Miscellaneous	B3-R/W,o-RO	01h
7Fh	Hidden Revision ID	--	--
80h~83h	Level 0 DRAM Sequencer DRAM Master Slice and Latency Control	R/W	B7530731h
84h~87h	Level 1 DRAM Sequencer DRAM Master Slice and Latency Control	R/W	E1100731h
88h	Level 0 DRAM Sequencer Arbitration Control	R/W	00h
89h	Level 1 DRAM Sequencer Arbitration Control	R/W	01h
8Ah	Memory Interface Clock Gated Control	R/W	20h
8Bh	DRAM Write Buffer Control	R/W	00h
8Fh-8Ch	Reserve	R/W	x00000000h

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(continued)

Host Interface and CPU Decode Configuration Register			
90h	C Segment Shadow Control Register	R/W	00h
91h	D Segment Shadow Control Register	R/W	00h
92h	E Segment Shadow Control Register	R/W	00h
93h	SMM Control Register	R/W	00h
94h	Memory Gap 0 Size Register	R/W	00h
95h	Memory Gap 0 Base Register	R/W	00h
96h	Memory Gap 1 Size Register	R/W	00h
97h	Memory Gap 1 Base Register	R/W	00h
98h	Memory/IO Range Control Register	R/W	00h
99h	Latch Control Signal Register H	R/W	00h
9Ah	Latch Control Signal Register M	R/W	
9Bh	Post Write Control Register	R/W	
9Ch	CPU Interface Control Register	_,R/W	20h
9Dh	Host Clock and Memory Clock Interface Control Register	RO,R/W	
9Eh	Host to Memory read Enhance Control Register		
9Fh	Reserve		

(continued)

PCI Power Management Enable (PME) Configuration Registers			
A0h~A3h	Power Management Control Block #2 – Starting Address	R/W	--
A4h	Power Management Capability Identifier Register	R/W lock	--
A5h	Power Management Next Item Pointer Register	R/W Lock	--
A6h~A7h	Power Management Capabilities Register	R/W lock	0001h
A8h~A9h	Power Management Control and Status Register	R/W lock	0000h
AAh	PMCSR PCI to PCI bridge Support Extensions	R/W lock	00h
ABh	Data Register	R/W lock	00h
ACh~AFh	Reserve	--	--
A.G.P. GART/GTLB Configuration Registers			
B0h~B3h	A.G.P. Capability Identifier Register.	R/W lock	00
B4h~B7h	A.G.P. Status Register.	R/W lock	00
B8h~BBh	A.G.P. Command Register	R/W	00
BCh~BFh	GART Base Address and NLVM Size	R/W	00h
C0h~C3h	Level2 GTLB Control	R/W	10130000h
C4h~C7h	GTLB Control	R/W	00h
C8~CBh	A.G.P. Control Register Two	R/W	00h
CCh~CFh	GTLB TAG Status	R/W	00h
Bus Interface Timing Control Registers			
D0h	Global Gated Clock Control	R/W	00h
D1h	Memory Interface Timing Compensation Control I	R/W	F0h
D3h-D2h	Memory Interface Timing Compensation Control II	R/W	FF58h
D7h – D4h	Memory Interface I/O driver control and Memory Interface DLL/process-monitor status report register	R/W, RO	00000000h
D8h	NB CPU_INFX PLL Reserved Register	R/W	
D9h	NB CPU_INFX PLL Control Register		40h
DAh	Host Data Output 400MHz Clock Delay Line	R/W	1Ah
DBh	NB Frequency Interface Control Register		00h
DCh	NB Host PLL Control Register		
DDh	NB Memory PLL Control Register		80h
DEh	NB AGP PLL Control Register		80h
DFh	Other NB PLL Control Register		00h
E3h-E0h	Memory Interface DDR-SDRAM DDLL 1/4T delay generator control	R/W	39002C00h
E7h~E4h	Memory Interface DDR SDRAM output (write)-path DLL configuration	R/W	2F3B0040h
E8h~EBh	AGP DLL Control Register	R/W	00040002h
ECh~EFh	AGP I/O Pad Tracking Circuit Control	R/W	00
F0h	CPU STB_IN Delay Selection Register	R/W	00
F1h	CPU I/O DLL Status Register	R/W	00h
F2h	CPU DLL Soft Mode Register	R/W	00h
F3h	CPU DLL Status Register	RO	
F4h-F5h	NB Addr/Data STBPJ/STBNJ Delay Line Control	R/hw setting	
F6h	NB CPU_INFX_DLL_COMP_Out	RO	
F7h	Reserve		00h
F8h-F9h	Configuration Registers Reserved for BIOS use	R/W lock	
Fah	Real Revision ID and Revision ID	R/W lock	
FBh	Real Revision ID and Revision ID	R/W lock	
FCh-FFh	Configuration Registers Reserved for BIOS use	R/W	0000h

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Offset 0CFFh-0CFCh: Configuration Data Register

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 00-01h
Register Name: **Vender Identification Register**
Attribute : Read
Default Value : 10B9h

Bit	Description
15:0	This is a 16-bit value assigned to Acer Laboratories Inc.

Register Index: Index 02-03h
Register Name: **Device Identification Register**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah
Default Value 1671h

Bit	Description
15:0	This is a 16-bit value assigned to M1671 of Acer Laboratories Inc.

Register Index: Index 04-05h
Register Name: **Command Register**
Attribute : Read/Write

Bit	Description
15:10(000000)	Reserve
9(0)	Fast Back-to-Back Enable
8(0)	SERR# Enable This bit is an enable bit for the SERR# driver. A value of 0 disables SERR# driver. A value of 1 enables the SERR# driver.
7(0)	Write Cycle Enable
6(0)	Parity Error Response. When the bit is set, the host bridge will take its normal action when a parity error is detected. When the bit is 0, the host bridge will ignore any parity errors that it detects and continue normal operation.
5(0)	VGA Palette Snoop Enable
4(0)	Memory Write and Invalidate Enable
3(0)	Special Cycle Recognition
2(0)	Master Enable. Controls host bridge's ability to act as a master of PCI Bus. This bit should be set by BIOS after RESETJ is deasserted.
1(0)	Memory Space Enable. Controls host bridge's response to memory space accesses. A value of 0 disables the host bridge response. A value of 1 allows the device to respond to memory space access. This bit should be set by BIOS after RESETJ is deasserted.
0 (0)	I/O Access Enable

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 06-07h
Register Name: **Status Register**
Attribute : Read/Write

Bit	Description
15(0)	Detected Parity Error. The host bridge will set this bit whenever it detects a parity error, even if parity error handling is disabled.
14(0)	Signaled System Error The host bridge will set this bit when it asserts SERR#.
13(0)	Received Master Abort The host bridge will set this bit when its transaction is terminated with Master-Abort.
12(0)	Received Target Abort The host bridge will set this bit when its transaction is terminated with Target-Abort.
11(0)	Signal Target Abort
10:9(01)	DEVSEL timing The host bridge is fixed to medium decode
8 (0)	Data Parity Error Detected It will be set when three conditions are met 1) the host bridge setting the bit acted as the bus master for the operation; 2) the host bridge asserted PERR# itself or observed PERR# asserted; 3) The Parity Error Response bit is set.
7(0)	Fast Back-to-Back Capable
6(0)	UDF (User Definable Feature) Supported
5 (0)	66MHz-Capable
4 (1)	AGP capabilities pointer bit This bit means the M1671 has implemented the function of Accelerated Graphic Port. Attribute: Read/Lock Write controlled by Bit4 of Index 4Ah
3:0(0h)	Reserve

Register Index: Index 08h
Register Name: **Revision Identification Register**
Attribute: Read/ Lock Write controlled by Bit4 of Index 4Ah
Default Value 00h

Bit	Description
7:0	This is an 8-bit value that indicates the revision identification number for M1671 of ALi.

Register Index: Index 09h
Register Name: **Specific Register-level Programming Register**
Attribute: Read
Default Value 00h

Bit	Description
7:0	This value of M1671 is 00h.

Register Index: Index 0Ah
Register Name: **Sub-Class Code Register**
Attribute: Read
Default Value 00h

Bit	Description
7:0	This value of M1671 is 00h.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 0Bh
Register Name: **Base-Class Code Identification Register**
Attribute: Read
Default Value: 06h

Bit	Description
7:0	The value of M1671 is 06h. It means the M1671 is a Host Bridge device.

Register Index: Index 0Ch
Register Name: **Cache Line Size**
Attribute : Read
Default Value : 00h

Bit	Description
7:0	Cache Line Size Register

Register Index: Index 0Dh
Register Name: **Latency Timer**
Attribute : Read
Default Value : 00h

Bit	Description
7:0	Latency Timer Register

Register Index: Index 0Eh
Register Name: **Header Type**
Attribute : Read
Default Value 00h

Bit	Description
7:0	Header Type Register

Register Index: Index 0Fh
Register Name: **BIST (built-in self test)**
Attribute : Read
Default Value 00h

Bit	Description
7:0	Built-in Self Test Register

Register Index: Index 10-13h
Register Name: **Base Address Register**
Attribute : Read/Write
Default Value 00000008h

Bit	Description
31:0	This is a memory base register of M1671. The address type is 32-bit address space and the data of the memory space is prefetchable. This memory space is located for Non-Local Video Memory of AGP function. The memory space is controlled by bit[3:0] of index BCh.

Register Index: Index 14-17h
Register Name: **Base Address Register**
Attribute : Read
Default Value : 00000000h

Bit	Description
31:0	Base Address Register

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 18-1Bh
Register Name: **Base Address Register**
Attribute : Read
Default Value : 00000000h

Bit	**Description**
31:0	Base Address Register

Register Index: Index 1C-1Fh
Register Name: **Base Address Register**
Attribute : Read
Default Value : 00000000h

Bit	**Description**
31:0	Base Address Register

Register Index: Index 20-23h
Register Name: **Base Address Register**
Attribute : Read
Default Value : 00000000h

Bit	Description
31:0	Base address Register

Register Index: Index 24-27h
Register Name: **Base Address Register**
Attribute : Read
Default Value 00000000h

Bit	Description
31:0	Base Address Register

Register Index: Index 28-2Bh
Register Name: **CardBus CIS Pointer**
Attribute : Read
Default Value 00000000h

Bit	Description
31:0	Cardbus CIS Pointer

Register Index: Index 2C-2Dh
Register Name: **Subsystem Vendor ID**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah
Default Value 0000h

Bit	**Description**
15:0	Subsystem Vendor ID

Register Index: Index 2E-2Fh
Register Name: **Subsystem ID**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah
Default Value 0000h

Bit	**Description**
15:0	Subsystem ID

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 30-33h
Register Name: **Expansion ROM Base Address**
Attribute : Read
Default Value 00000000h

Bit	Description
31:0	Expansion ROM Base Address

Register Index: Index 34h
Register Name: **Capabilities Pointer Register**
Attribute: Read/ Lock Write controlled by Bit4 of Index 4Ah
Default Value B0h

Bit	Description
7:0	This register contains a byte offset into the host bridge's configuration space containing the fist item in the capabilities list and is a read only register. The first capability of M1671 is AGP and the byte offset is B0h.

Control Registers for Primary PCI bus

Register Index: Index 40h
Register Name: **Control Register of PCI bridge execution mode**
Attribute : Read/Write

Bit	Description
7:5(000)	Reserve
4(1)	The enable bit for retrying CPU while PCI bus stall too long. Time out counter is defined in x41[7:0] based on PCLK. 0 : Disable 1: Enable
3(1)	The enable bit for Secondary PCI bridge to defer current cycle when followed by a Primary PCI cycle in dynamic defer mode 0 : Disable 1 : Enable
2(1)	The enable bit for Primary PCI bridge to defer current cycle when followed by a Secondary PCI cycle in dynamic defer mode 0 : Disable 1 : Enable
1(0)	Debug mode and reserved for north bridge 0 : Disable 1 : Enable
0(1)	CPU to PCI Bridge Execution Mode. 0 - Synchronous Mode, 1 - Dynamic Defer Mode

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 41h
Register Name: **Stall Retry Counter**
Attribute : Read/Write
Default Value 2Fh

Bit	Description
7:0	Value for Stall Retry Counter according to 40 bit[4]

Register Index: Index 42h
Register Name: **Control Register for Posted Write of Primary PCI bridge**
Attribute : Read/Write

Bit	Description
7(0)	Reserve
6:4(000)	PCI Post Write Enhance Option of PCI33 000 – Disable post write enhance 011 – Enable post write turbo 111 – Enable post write bypass others – Reserve.
3(1)	The enable bit for performing posted-write function. 0 - Disable 1 – Enable
2(1)	The select bit for performing posted-write function in USWC region or all memory regions. 0 - USWC Region 1 - All Memory Regions
1(1)	CPU to PCI/AGP Read cycle wait for PCI Master write buffer empty 0 - Disable 1 – Enable
0(1)	Enable bit for PCI Master wait flushing deferred reply cycles in In-Bound-Queue when synchronous mode.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 43h
Register Name: **Special Cycle**
Attribute : Read/Write

Bit	Description
7(1)	Test bit and reserved for north bridge.
6(0)	Reserve
5(0)	Support decoding of 64-bit IO cycles 0 - Disable 1 – Enable
4(0)	Latch block enable 0 - Disable 1 – Enable
3:1(000)	Reserve
0(0)	Special cycle mode In basic mode, Only Shutdown, Halt and StopGrant special cycle will appear at PCI bus. In advanced mode, Special cycle issued from CPU will all transfer to PCI bus. 0 : Basic Mode 1 : Advanced Mode

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 44h
Register Name: **Control Register I for PCI Slave**
Attribute : Read/Write

Bit	Description
7 (0)	Decode PCI Read-Multiple Command 0 : Disable 1 : Enable
6:4 000 (One line mode)	Prefetch Prediction for PCI Read Line/Multiple command for P4 systems: 000,001 - One Line mode (16 Double Word) 010,011 - Dual line mode (32 Double Word) 1XX - Not Supported
3:2(00)	00: No maximum latency control, wait forever 01: Support 64+8 Latency control 10: Support 32+8 Latency control 11: No support
1(0)	Delayed Transaction Function 0 - Disable, the PCI master read interface of M1671 will not perform Delayed-Transaction. 1 - Enable, the PCI master read interface of M1671 will perform Delayed-Transaction.
0(0)	Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 45h
Register Name: **Control Register 2 of PCI Slave function**
Attribute : Read/Write

Bit	Description
7:6(00)	Reserve
5(0)	Priority Queue
4(1)	Set to 1 for normal operation.
3(0)	Enable/Disable M1671 to issue PCI LOCK access. 0 - Disable 1 – Enable
2:1(00)	Reserve
0(0)	PCI DEVSEL# response timing, 0 - Medium, 1 - Slow.

Register Index: Index 46h
Register Name: **Counter for Primary PCI Delay Transaction**
Attribute : Read/Write
Default Value 04h

Bit	Description
7:0	This byte counter is for the aborting mechanism of Primary PCI Delay-Transaction. If the same PCI master device issue the different line boundary cycle after that the previous read cycle of itself been served as a delay transaction. If the number of different cycles is equal to this counter, the M1671 will abort the current delay transaction.

Register Index: Index 47h
Register Name: **PCI Bridge Retry Counter Register**
Attribute : Read/Write
Default Value 0Ah

Bit	Description
7:0	PCI retry counter. The maximum times that M1671 (PCIMST) will reissue the command on PCI bus when it is continuously retried. When the counter expires then M1671 will abort the command. A 00h value means to disable the Retry Counter, i.e. always retry until transaction completed on PCI bus. The M1671 will retry the cycle in host bus if this command is a Synchronous cycle. Or M1671 will return Defer-Retry cycle for defer mode cycle.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 48h
Register Name: **PCI Bridge Error Command Register**
Attribute : Read / Write-One-Clear

Bit	Description
7(0)	Reserve
6(0)	Issue SERR# when M1671 issue write cycle and receive PERR#. 0 - Disable 1 - Enable
5(0)	Issue SERR# on received Data Parity Error. 0 - Disable 1 – Enable
4(0)	Issue SERR# on Address Parity Error detecting. If enabled the M1671 will assert SERR# when detect a PCI address parity error. 0 - Disable 1- Enable
3(0)	Reserve
2(0)	When the Host-to-PCI cycle is terminated by Target-Abort, The M1671 will report SERR#. 0 - Disable 1 – Enable
1(0)	Assert SERR# for ECC Single-Bit Error 0 - Disable 1 – Enable
0(0)	Assert SERR# ECC Multiple-Bits Error 0 - Disable 1 – Enable

Register Index: Index 49h
Register Name: **PCI Bridge Error Status Register**
Attribute : Read

Bit	Description
7(0)	Reserve
6(0)	Detect SERR# when M1671 issue write cycle and receive PERR#.
5(0)	M1671 detects PCI Data Parity Error
4(0)	PCI Address Parity Error.
3:2(00)	Reserve
1(0)	Memory Data ECC Single-Bits Error.
0(0)	Memory Data ECC Multiple-Bits Error.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 4Ah
Register Name: **Control Register of Primary PCI master functional block**
Attribute : Read/Write

Bit	Description
7:6(11)	Test bits reserved for north bridge.
5(0)	PCI multi-function pad selection PREQJ[5]/AGP_BUSYJ, PGNTJ[5]/AGP_STOPJ. 0 : Select PREQJ[5], PGNTJ[5]. 1 : Select AGP_BUSYJ, AGP_STOPJ.
4(0)	Write control bit for Capabilities Pointer Register, P2P device ID, Host Bridge device ID, Subsystem ID, Subsystem Vendor ID, B1_reg capability pointer and Power Management A4_reg & A8_reg. When this bit is set, those registers can be written with any value. Otherwise, those registers are read-only. 0 - Disable, 1 - Enable.
3 (0)	Enable bit for PCI CLKRUN protocol. If this bit is enabled, SERRJ of PCI bus will be used as CLKRUN and compliant to CLKRUN protocol in PCI Mobile Design Guide. 0 - disable 1 – enable
2 (0)	When this bit is set, the PCI master will wait for all the internal command and data buffer to be empty, then the PCI master issues the Stop Grant, Halt and Shutdown special cycles. 0 - Disable 1 – Enable
1 (0)	This bit enables M1671 to transfer the shutdown special cycle to IO Port 92 write cycle. 0 - Disable 1 - Enable
0(0)	Reserve

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 4Bh
Register Name: **PCI Arbiter Control Register**
Attribute : Read/Write

Bit	Description
7(0)	PCI Arbiter Guarantee Access Mode 0 - disable 1 - enable, cycles pending in PCI-POST-WRITE will be flushed before grant are given to requesting masters
6(0)	The enable bit for locking PCI bus while PHOLDJ/PHLDAJ are both asserted 0 - Enable 1 – Disable
5(0)	In P4 Mode, when CPU issue lock cycle, control arbiter to grant bus ownership to north bridge 0 - Disable 1 – Enable
4(0)	Reserve.
3(0)	High Priority PCI Master Function Enable for 1394 card 0 - Disable 1 - Enable, the PCI device indicated in Bit[7:2] of Offset 4Ch will have higher priority than other PCI devices.
2(0)	Location of High Priority PCI device 4B(Bit[2]) & 4C(Bit[7:2]) => PCI Master 6-0
1(0)	ISA bridge Passive Release mode 0 - Disable 1 - Enable
0 (0)	Complete Bus Lock Function 0 - Disable 1 – Enable

Register Index: Index 4Ch
Register Name: **Primary PCI bus Arbiter Control Register**
Attribute : Read/Write

Bit	Description
7:2(000000)	Location of High Priority PCI device
1:0 (00)	The scaling factor for master time slice Primary PCI bus arbiter under Passive-Release mode 00 : divided by 2 01 : divided by 4 10 : divided by 8 11 : divided by 1

Register Index: Index 4Dh
Register Name: **PCI Master Device Multiple Transaction Time Slice**
Attribute : Read/Write
Default Value 20h

Bit	Description
7:0	The Time Slice for PCI master to issue multiple transactions.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 4Eh
Register Name: **PCI Bridge Multiple Transaction Time Slice**
Attribute : Read/Write
Default Value 20h

Bit	Description
7:0	Time Slice for M1671 to issue multiple transactions.

Register Index: Index 4Fh
Register Name: Reserve
Default Value 00h

Bit	Description
7:0	Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)
Control registers for Secondary PCI bus

Register Index: Index 50h
Register Name: **Control Register of Secondary PCI bridge execution mode**
Attribute : Read/Write

Bit	Description
7 (0)	Reserve
6:4 (000)	PCI post write enhance option of AGP 000: Disable post write enhance 011: enable post write turbo 111: enable post write bypass others: Reserve
3:1(000)	Reserve
0 (1)	Secondary PCI Bridge Side Execution Mode, 0 - Synchronous Mode 1 - Defer Mode

Register Index: Index 51h
Register Name: Reserve
Attribute : Read/Write

Bit	Description
7:0	Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 52h
Register Name : **PCI Gated Clock Control Registers**
Attribute : Read/Write

Bit	Description
7:4(0000)	0000: Enable AGP interface power saving mode of north bridge 1111: disable AGP interface power saving mode of north bridge
3:0(0000)	0000: Enable PCI interface power saving mode of north bridge 1111: disable PCI interface power saving mode of north bridge

Register Index: Index 53h
Register Name: Reserve
Attribute : Read/Write

Bit	Description
7:6(00)	Reserve
5(0)	Support decoding of 64-bit IO cycles 0 - Disable 1 - Enable
4:0(00000)	Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 54h
Register Name: **Control Register I for Secondary PCI Master Interface**
Attribute : Read/Write
Default Value : 01h

Bit	Description
7(0)	Decode PCI Read-Multiple Command 0 : Disable 1 : Enable
6:4 (000)	Prefetch Prediction for PCI Read Line/Multiple command for P4 system: 000,001 - One Line mode (16 double word) 010,011 - Dual line mode (32 double word) 1xx - Not supported
3:2 (00)	00: No maximum latency control, wait forever 01: Support 64+8 latency control 10: Support 32+8 latency control 11: no support
1 (0)	Delayed Transaction Function 0 - Disable, the PCI master read interface of M1671 will not perform Delayed-Transaction. 1 - Enable, the PCI master read interface of M1671 will perform Delayed-Transaction.
0 (1)	AGP Park enable. If all requests of AGP bus are deasserted, the AGP arbiter will park to north bridge 0 - Disable 1 - Enable

Register Index: Index 55h
Register Name: **Control Register II of Secondary PCI Master Interface**
Attribute : Read/Write
Default Value 10h

Bit	Description
7:5(000)	Reserve
4 (1)	Set to 1 for normal operation
3:1 (000)	Reserve
0 (0)	PCI DEVSEL# response timing 0: Medium 1: Slow

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 56h
Register Name: **Counter for Secondary PCI Delay Transaction**
Attribute : Read/Write
Default Value 04h

Bit	Description
7:0	This byte counter is for the aborting mechanism of Secondary PCI Delay-Transaction. If the same PCI master device issue the different line boundary cycle after that the previous read cycle of itself been served as a delay transaction. If the number of different cycles is equal to this counter, the M1671 will abort the current delay transaction.

Register Index: Index 57h
Register Name: **PCI Bridge Retry Counter Register**
Attribute : Read/Write
Default Value 2Fh

Bit	Description
7:0	PCI retry counter. The maximum times that the M1671 (PCI master) will reissue the command on Secondary PCI bus when it is continuously retried. A 00h value means to disable the Retry Counter, i.e. always retry until transaction completed on AGP bus. When the counter expires then M1671 will abort the command. The M1671 will then retry the cycle in host bus if this command entry is a Synchronous cycle. Or M1671 will return Defer-Retry cycle for defer mode cycle.

Register Index: Index 58h
Register Name: **PCI Bridge Error Command Register**
Attribute : Read/Write-One-Clear
Default Value 00h

Bit	Description
7 (0)	Reserve
6 (0)	Issue SERR# when M1671 issue write cycle and receive PERR#. 0 - Disable 1 – Enable
5 (0)	Issue SERR# on received Data Parity Error. 0 - Disable 1 – Enable
4 (0)	Issue SERR# on Address Parity Error detecting. If enabled the M1671 will assert SERR# when detect a PCI address parity error. 0 - Disable 1 – Enable
3 (0)	Assertion ability of Secondary PCI SERR# 0 - Disable 1 - Enable
2(0)	When the Host-to-Secondary PCI cycle is terminated by Target-Abort, the M1671 will report SERR#. 0 - Disable 1 - Enable
1:0 (00)	Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 59h
Register Name: **Secondary PCI Bridge Error Status Register**
Attribute : Read

Bit	Description
7 (0)	Reserve
6 (0)	Detect PERR# when M1671 issue write cycle and receive PERR#.
5 (0)	M1671 detect Secondary PCI Data Parity Error
4 (0)	Secondary PCI Address Parity Error
3:0(0000)	Reserve

Register Index: Index 5Ah
Register Name: **Control Register of Secondary PCI Bridge**
Attribute : Read/Write
Default Value: 00h

Bit	Description
7:0	Reserve

Register Index: Index 5Bh-5Ch
Register Name: Reserve
Attribute : Read/Write

Register Index: Index 5Dh
Register Name: **Secondary PCI Master Device Multiple Transaction Time Slice**
Attribute : Read/Write
Default Value 20h

Bit	Description
7:0	The Time Slice for Secondary PCI master to issue multiple transactions.

Register Index: Index 5Eh
Register Name: **Secondary PCI Bridge Multiple Transaction Time Slice**
Attribute : Read/Write
Default Value 20h

Bit	Description
7:0	The Time Slice for M1671 to issue multiple transactions to Secondary PCI bus.

Register Index: Index 5Fh
Register Name: **DXI/DXO Multiple Transaction Time Slice**
Attribute : Read/Write
Default Value 20h

Bit	Description
7:0	The Time Slice for DXI(AGP read)/DXO(AGP write) to receive/provide data.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 60h
Register Name: **P4 write order control**
Attribute : [7:5]:Read only [4:0]:Read/Write

Bit	Description
7 (0)	Reserve
6 (0)	Reserve
5 (0)	Reserve
4 (0)	Write data transfer in order 0 : disable 1 : enable
3:0 (0000)	Reserve

Register Index: Index 61h
Register Name: Reserve
Attribute : Read/Write
Default Value 00h

Bit	Description
7:0	Reserve

Register Index: Index 62h
Register Name: **Host IO pad driving capability status register**
Attribute : Bit[7:2] Read Only, Bit[1:0] Read/Write

Bit	Description
7:2 (auto detect)	Record IO pad driving capability from Tracing Circuit 0 : turn off 1 : turn on Bit[7] : HTRC_N4X Bit[6] : HTRC_N2X Bit[5] : HTRC_N1X Bit[4] : HTRC_T4X Bit[3] : HTRC_T2X Bit[2] : HTRC_T1X
1:0	Reserve

Register Index: Index 63h
Register Name: **Host IO driving capability control register**
Attribute : Bit[7:1] Read Only, Bit[0] Reserve

Bit	Description
7:2 (auto detect or hw setting)	Record final status of IO driving capability 0 : turn off 1 : turn on Bit[7] : DRIVE_N4X Bit[6] : DRIVE_N2X Bit[5] : DRIVE_N1X Bit[4] : DRIVE_T4X Bit[3] : DRIVE_T2X Bit[2] : DRIVE_T1X
1	Control the determination of IO driving capability 1 : sample from Tracing circuit 0 : sample from HW Setting
0	CPU ILL PMOS termination enable 0: switch PMOS off 1: switch PMOS on

NOTE : 1. The driving capability could be set from XADJ[14:12]/XADJ[17:15] for N/T
if Bit[1] is set to 0. Bit[1] is set from XADJ[11].
For details, please refer to power-up sequence document.

Register Index: Index 64h-6Fh
Register Name: **Host to memory frequency interface control**
Attribute : Read/Write
Please keep default value for normal operation (or refer to BIOS Programming Guide)

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 71h-70h(DIMM0) 73h-72h(DIMM1) 75h-74h(DIMM2)
Attribute : Read/Write
DIMM memory module/device specific parameters. 1 bytes for each ROW. A ROW is defined to be a set of DRAM devices in a DIMM that uses the same CSJ (chip-select) signal driven by the memory controller.

Bit	Description
7:6	Specify the device bank address type(BA type) 00 : ROW not present 01 : 1 bit (2-bank devices) 1x : 2 bit (4-bank devices) Default : "10" for row0, "00" for others.
5:3(000)	Specify the DRAM Device Column Address width. 000 : 8 bit 001 : 9 bit 010 : 10 bit 011 : 11 bit 1xx : 12 bit
2:0 (010)	Specify the "ROW SIZE"(in unit of Mega-Byte) for this DIMM module.

Supported Device Organization			Address Width(no. of bit)						
			BA	RA	CA		BA	RA	CA
000			Reserve						
001			Reserve						
010	32MB	16Mbx4	1	11	10				
	32MB	64Mbx16	2	12	8	or	1	13	8
	32MB	128Mbx32	2	12	8				
011	64MB	64Mbx8	2	12	9	or	1	13	9
	64MB	128Mbx16	2	12	9	or	2	13	8
	64MB	256Mbx32	2	12	9	or	2	13	8
100	128MB	64Mbx4	2	12	10	or	1	13	10
	128MB	128Mbx8	2	12	10	or	2	13	9
	128MB	256Mbx16	2	12	10	or	2	13	9
	128MB	512Mbx32	2	13	9				
101	256MB	128Mbx4	2	12	11	or	2	13	10
	256MB	256Mbx8	2	12	11	or	2	13	10
	256MB	512Mbx16	2	13	10				
110	512MB	256Mbx4	2	13	11				
	512MB	512Mbx8	2	13	11				
111	1GB	512Mbx4	2	13	12				

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 76h
Register Name: **DRAM DIMM type/Gated Clock Global Configuration**
Attribute : Read/Write

Bit	Description
7 (0)	MBIU gated-clock control. Force the MBIU clock to be stopped when idle for more than 8 clocks. 0 : disable 1 : enable
6 (0)	Deassert CKE[5:0] when MBIU clock is stopped for saving DRAM power.(Active power down) 0 : disable 1 : enable
5 (0)	Reserve. Please keep 0 for normal operation.
4 (0)	Suspend all the North-Bridge I/O pads(except clocks, resetj, suspendj, mem-side signals) during ACPI S1 or S3. 0 : disable (save mode for ACPI S1) 1 : enable (required for ACPI S3)
3 (0)	ACPI S3 CKE waking up policy. 0 : Wake-up CKE automatically by hardware. 1 : CKE wake-up by software. Software(BIOS) wakeup the CKE by applying a sequence of clearing and then setting this bit.
2:0 (000)	DIMM/Memory type global setting 000 : unbuffered DIMM with JEDEC standard SDRAM(SDR) 001 : Reserve 010 : Reserve 011 : Reserve 1xx : unbuffered DIMM with JEDEC DDR SDRAM(DDR)

Register Index: Index 77h
Register Name: **Advanced Power-Saving Mode Control Register**
Attribute : Read/Write
Default Value 00h

Bit	Description
7 (0)	SDRAM self-refresh mode after CPU issues HALT special cycle. 0 : disable. Keep the DRAM in normal operation. 1 : enable. The DRAM enters self refresh mode.
6 (0)	SDRAM self-refresh mode after idle-timer timed-out. 0 : disable. Keep the DRAM in normal operation. 1 : enable. The DRAM enters self refresh mode.
5:4(00)	SDRAM idle timer for self refresh. 00 : 16 us 01 : 32 us 10 : 64 us 11 : 128 us
3:0	Reserve.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 78h
Register Name: **MBIU Global Configuration**
Attribute : Read/Write

Bit	Description
7:6 (00)	Memory address/command setup time before CSJ being sampled asserted. 00 : 3T 01 : 2T 1x : 1T
5:3 (000)	Special/Configuration mode (for DRAM initialization). Under special mode, all CPU to DRAM "read" cycles will be translated to MBIU special mode cycles and one of the following mode-command specified will be executed. Note: Write command (to DRAM) is not supported under special mode. Issuing DRAM write cycles under special mode will result in undefined operations. 000 : disabled (normal operation) 001 : drive the command "NOP" on the command bus. 010 : SDRAM Pre-charge All command 011 : SDRAM Mode Register Load command 100 : Auto Refresh command 101 : Reserve 110 : Reserve 111 : Reserve
2:0 (000)	Internal debugging mode only, set to '000' for normal operation.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 79h
Register Name: **MBIU/DataPath Global Setting**
Attribute : Read/Write

Bit	Description
7(0)	2T data turnaround between read and write 0 : 2T turnaround 1 : 1T turnaround
6(0)	Memory command bus idle-park. 0 : Idle park at NOP command. This is safe mode. 1 : Idle park on CAS READ/RAS command depends on bank-opening status selecting this mode will boost the performance.
5:4 (01)	CAS read latency[1:0] for DDR/SDR SDRAM. Note: These 2 bits describing DDR or SDR depends on the DIMM type specified. 00 : 1.5(DDR), 2(SDR) 01 : 2.0(DDR), 2(SDR) 10 : 2.5(DDR), 3(SDR) 11 : Reserve(DDR), 3(SDR)
3:1(000)	DDR read-path latency control. 000 : normal latency mode 001 : short latency mode 01x : Reserve 10x : X.5 Enhanced Latency mode II 11x : X.5 Enhanced Latency mode I
0(0)	DDR read cycle safe mode. In safe mode, the MBIU will prevent any 2 successive read CSJs from being 3T apart. This is a workaround for avoiding the DQS glitch problem during one-wait read to read case. 0 : disable 1 : enable

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 7Ah
Register Name: **DRAM Basic Timing Control Register**
Attribute : Read/Write

Bit	Description
7:5 (000)	tRAS value in unit of mclk cycle. range from 3 to 10. 000 : 10T 001 : 9T 010 : 8T 011 : 7T 100 : 6T 101 : 5T 110 : 4T 111 : 3T
4:3 (00)	RAS to CAS delay timing in unit of mclk cycle. 00 : 5T 01 : 4T 10 : 3T 11 : 2T
2:0 (000)	tRP value in unit of mclk cycle, range is from 2 to 9. 000 : 9T 001 : 8T 010 : 7T 011 : 6T 100 : 5T 101 : 4T 110 : 3T 111 : 2T

Register Index: Index 7Bh
Register Name: **Misc/Paging Control**
Attribute : Read/Write

Bit	Description
7 (0)	Reserved for chipset internal debugging purpose. Please keep 0 for normal operation.
6:5 (00)	Turnaround between Last Write Data phase to the following "precharge" Command.(tDPL or tWR) 00 : 4T 01 : 3T 10 : 2T 11 : 1T
4 (0)	Enhanced Page Mode. Enabling this bit will force all the open pages to be closed when PLT (page-life-timer) expired. 0 : disable (Open Page Mode) 1 : enable
3:2 (00)	Page_life_time counter preset value for Enhanced Page Mode function. The counter will be preset on each CAS READ/WRITE access. 00 : 16 clocks 01 : 32 clocks 10 : 64 clocks 11 : 128 clocks
1:0 (00)	Refresh Queue Function Control 00 : Disable 01 : Queue depth=2 10 : Queue depth=4 11 : Queue depth=8

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 7C-7Dh
Register Name: **MBIU Refresh Control Register**
Attribute : Read/Write

Bit	Description
15: (0)	DRAM Refresh 0 : enable 1 : disable
14 (0)	Refresh Stagger 0 : disable 1 : enable
13:11 (000)	Default refresh CFGs[2:0] 000 : 410h*2 clocks, 15.6us when MCLK is 133MHz 001 : 30Ch*2 clocks, 15.6us when MCLK is 100MHz 010 : 208h*2 clocks, 7.8us when MCLK is 133MHz, 15.6us when MCLK is 66MHz 011 : 186h*2 clocks, 7.8us when MCLK is 100MHz 1xx : Using REFRESH_CNT[10:0] as preset value.
10:0	REFRESH_CNT[10:0], refresh counter preset value when Default refresh CFG="1xx"

Register Index: Index 7Eh
Register Name: **Miscellaneous**
Attribute : Read/Write

Bit	Description
7 (0)	Reserve.
6 (0)	Reserve. Keep 0 for normal operation.
5 (0)	Reserve.
4 (0)	184 pins SDRAM mode 0 : disable 1 : enable
3 (0)	Reserve
2 (0)	MBIU read data sync-in bypass 0 : disable 1 : enable
1 (0)	MBIU command/data sync-out bypass 0 : disable 1 : enable
0 (1)	MBIU Hardwired configuration bits write control. 0 : unlocked, read/write. 1 : locked, read only.

Register Index: Index 7Fh
Register Name: **M1671 Hidden Version ID**
Attribute : Read/Write Locked

Bit	Description
7:0	'00' for A0A

HOST-to-PCI BRIDGE (Bus 0, Device 0)
Memory Sequencer Configuration Register

Register Index: Index 80h~83h
Register Name: **Level0 DRAM Sequencer DRAM Master Slice and Latency Control**
Attribute : Read/Write
Default : B7530731h

Bit	Description
31:28	Global Memory Write Buffer Latency Timer. This timer defines the maximum request latency. It will count with the MWB request and sequencer does not respond. When this timer times-out, the MWB's request will become high priority to the arbiter of memory sequencer. "0000" : 4 Memory Clocks "0001" : 8 Memory Clocks . "1110" : 60 Memory Clocks "1111" : Never latency out
27:24	AGP Read Request Latency Timer.
23:20	Reserve.
19:16	CPU/PCI Read Request Latency Timer.
15:12	Global Memory Write Buffer (GMWB) command slice. Define the minimum number of commands that the memory sequencer will service the GMWB continuously. "0000" : 2 commands "0001" : 4 commands . "1110" : 30 commands "1111" : Never slice out
11:8	Reserve.
7:4	AGP Read Command Slice.
3:0	CPU/PCI Read command slice.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 84h~87h
Register Name: **Level1 DRAM Sequencer DRAM Master Slice and Latency Control**
Attribute : Read/Write
Default : E1100731h

Bit	Description
31:28	Reserve.
27:24	Reserve.
23:20	Level0 Sequencer Access Latency Timer in Level-1 Sequencer
19:16	GART Fetch Latency Timer in level-1 sequencer.
15:12	Reserve.
11:8	Reserve.
7:4	Level0 Sequencer Access Command Slice.
3:0	GART Fetch Command Slice.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 88h
Register Name: **Level0 DRAM Sequencer Arbitration Control**
Attribute : Read/Write
Default : 00h

Bit	Description
7	WBUF Request Priority Check 0 : Enable 1 : Disable
6	Reserve.
5	AGP Read Priority Check 0 : Enable 1 : Disable
4	CPU/PCI Read Priority Check 0 : Enable 1 : Disable
3:2	Reserve.
1:0	Arbitration sequence between masters. '00' : CPU/PCI Read -> AGP Read -> WBUF '01' : AGP Read -> CPU/PCI Read -> WBUF '10' : WBUF -> CPU/PCI Read -> AGP Read '11' : Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 89h
Register Name: **Level1 DRAM Sequencer Arbitration Control**
Attribute : Read/Write
Default : 01h

Bit	Description
7-6	Reserve.
5	Level0 Master Priority Check 0 : Enable 1 : Disable
4	GART Fetch Priority Check 0 : Enable 1 : Disable
3:2	Reserve.
1:0	Arbitration sequence between masters. '00' : GART fetch -> Level0 '01' : Level0 -> GART fetch '10' : Reserve '11' : Reserve

Register Index: Index 8Ah
Register Name: **Memory Interface Clock Gated Control**
Attribute : Read/Write
Default Value: 00h

Bit	Description
7	Memory Sequencer Clock Gated Function 0 : Disable 1 : Enable
6	GTLB Clock Gated Function 0 : Disable 1 : Enable
5	Memory Configuration Clock Gated Function 0 : Disable 1 : Enable
4:1	Reserve.
0	Memory Sequencer Bypass Mode 0 : Disable 1 : Enable

HOST-to-PCI BRIDGE (Bus 0, Device 0)
DRAM Global Write Buffer Configuration Register

Register Index: Index 8Bh
Register Name: **DRAM Write Buffer Control**
Attribute : Read/Write
Default : 00h

Bit	Description
7	Reserve.
6:4	Defines the times between the write-buffer-valid to write-buffer-flushing 000 : after 8 Memory clocks 001 : after 16 Memory clocks 010 : after 32 Memory clocks 011 : no time out flush 1xx : zero-delay flush
3	When this bit = 1, most of the flip-flops will be clock-gated when not used 0 : GATED CLOCK Disable 1 : GATED CLOCK Enable
2	Enable the write-same-page-first operation to enhance DRAM page hit rate 0 : enable write-same-page-first operation 1 : disable write-same-page-first operation
1:0	Reserve.

HOST-to-PCI BRIDGE (Bus 0, Device 0)
Frame Buffer Interface Configuration Register

Register Index: Index 8F-8Ch
Register Name: Reserve. Keep default value for normal operation
Attribute : Read/Write
Default : 00000000h

Bit	Description
23: 0	Reserve.

Host Interface and Pentium4 Series CPU Configuration Register

Register Index: Index 90h
Register Name: **C Segment Shadow Control Register**
Attribute : Read/Write

Bit	Description
7(0)	0CC000h-0CFFFFh shadow write enable 0 : disable 1 : enable
6(0)	0CC000h-0CFFFFh shadow read enable 0 : disable 1 : enable
5(0)	0C8000h-0CBFFFh shadow write enable 0 : disable 1 : enable
4(0)	0C8000h-0CBFFFh shadow read enable 0 : disable 1 : enable
3(0)	0C4000h-0C7FFFh shadow write enable 0 : disable 1 : enable
2(0)	0C4000h-0C7FFFh shadow read enable 0 : disable 1 : enable
1(0)	0C0000h-0C3FFFh shadow write enable 0 : disable 1 : enable
0(0)	0C0000h-0C3FFFh shadow read enable 0 : disable 1 : enable

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 91h
Register Name: **D Segment Shadow Control Register**
Attribute : Read/Write

Bit	Description
7 (0)	0DC000h-0DFFFFh shadow write enable 0 : disable 1 : enable
6 (0)	0DC000h-0DFFFFh shadow read enable 0 : disable 1 : enable
5 (0)	0D8000h-0DBFFFh shadow write enable 0 : disable 1 : enable
4 (0)	0D8000h-0DBFFFh shadow read enable 0 : disable 1 : enable
3 (0)	0D4000h-0D7FFFh shadow write enable 0 : disable 1 : enable
2 (0)	0D4000h-0D7FFFh shadow read enable 0 : disable 1 : enable
1 (0)	0D0000h-0D3FFFh shadow write enable 0 : disable 1 : enable
0 (0)	0D0000h-0D3FFFh shadow read enable 0 : disable 1 : enable

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 92h
Register Name: **E Segment Shadow Control Register**
Attribute : Read/Write

Bit	Description
7(0)	0EC000h-0EFFFFh shadow write enable 0 : disable 1 : enable
6(0)	0EC000h-0EFFFFh shadow read enable 0 : disable 1 : enable
5(0)	0E8000h-0EBFFFh shadow write enable 0 : disable 1 : enable
4(0)	0E8000h-0EBFFFh shadow read enable 0 : disable 1 : enable
3(0)	0E4000h-0E7FFFh shadow write enable 0 : disable 1 : enable
2 (0)	0E4000h-0E7FFFh shadow read enable 0 : disable 1 : enable
1 (0)	0E0000h-0E3FFFh shadow write enable 0 : disable 1 : enable
0 (0)	0E0000h-0E3FFFh shadow read enable 0 : disable 1 : enable

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 93h
Register Name: **SMM Control Register**
Attribute : Read/Write

Bit	Description
7:6 (10)	SMM memory accessing address selection 00 : D0000h-DFFFFh -> B0000h-BFFFFh 01 : A0000h-BFFFFh 10 : 30000h-3FFFFh -> B0000h-BFFFFh 40000h-4FFFFh -> A0000h-AFFFFh 11 : C0000h-CFFFFh -> A0000h-AFFFFh D0000h-DFFFFh -> B0000h-BFFFFh
5 (0)	Only fetch cycle can access SMM memory 0 : disable, no matter code or data cycle, SMM memory can be access 1 : enable
4 (0)	Normal cycle access SMM memory 0 : disable, only when SMIACTJ is active, SMM memory can be access 1 : enable, no matter if SMIACTJ is active, SMM memory can be access
3(0)	SMM memory allowance 0 : disable, 93:7-4 have no effects 1 : enable
2(0)	0A0000h-0BFFFFh memory cycle pass to DRAM 0 : disable, 0A0000h-0BFFFFh memory cycle pass to PCI/AGP 1 : enable, 0A0000h-0BFFFFh memory cycle pass to DRAM note: This bit is useful only when reg93h[7:3] is failing
1(0)	0F0000h-0FFFFFh shadow write enable 0 : disable 1 : enable
0 (0)	0F0000h-0FFFFFh shadow read enable 0 : disable 1 : enable

Register Index: Index 94h
Register Name: **Memory Gap 0 Size Register**
Attribute : Read/Write

Bit	Description
7:4 (0000)	PCI33 memory gap 0 base address 23-20.
3(0)	PCI33 memory gap 0 USWC mode enable 0 : disable 1 : enable, if memory cycle fall in memory gap 0, no matter what attribute come with the cycle, always treat this cycle as post write cycle.
2:0 (000)	PCI33 memory gap 0 size 000 : 1MB 001 : 2MB 010 : 4MB 011 : 8MB 100 : 16MB 101 : 32MB 110 : 64MB 111 : Reserve

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 95h
Register Name: **Memory Gap 0 Base Register**
Attribute : Read/Write
Default Value : 00h

Bit	Description
7:0	PCI33 memory gap 0 base address 31-24.

Register Index: Index 96h
Register Name: **Memory Gap 1 Size Register**
Attribute : Read/Write
Default Value 00h

Bit	Description
7:4	PCI33 memory gap 1 base address 23-20.
3	PCI33 memory gap 1 USWC mode enable 0 : disable 1 : enable, if memory cycle fall in memory gap 1, no matter what attribute come with the cycle, always treat this cycle as post write cycle.
2:0	PCI33 memory gap 1 size 000 : 1MB 001 : 2MB 010 : 4MB 011 : 8MB 100 : 16MB 101 : 32MB 110 : 64MB 111 : Reserve

Register Index: Index 97h
Register Name: **Memory Gap 1 Base Register**
Attribute : Read/Write
Default Value 00h

Bit	Description
7:0	PCI33 memory gap 1 base address 31-24.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 98h
Register Name: **Memory/IO Range Control Register**
Attribute : Read/Write

Bit	Description
7 (0)	High I/O address mask control. 0 : disable, A[31:16] of I/O request will be passed as received 1 : enable, A[31:16] of I/O request will be masked as 0
6 (0)	ISA I/O address aliasing control. 0 : disable 1 : enable, if I/O request address A[9:8] are not both 0, A[15:10] will be aliased to 0.
5 (0)	If enabled, P2P bridge will monitor 3C6h, 3C8h and 3C9h, I/O write cycle and issue it to secondary PCI bus. 0 : disable 1 : enable
4(0)	Monochrome Device Adapter presence at PCI. If enabled, the following standard MDA resources will be directed to PCI bus memory : 0B0000h-0B7FFFh I/O : 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh. 0 : disable 1 : enable
3(0)	CPU/PCI master issue memory cycle which address fall in NLVM will be passed to DRAM (translated by GART) 0 : disable 1 : enable
2(0)	Memory cycle which address fall in 0A0000h-0BFFFFh, no matter what attribute come with the cycle, always treat this cycle as post write cycle 0 : disable 1 : enable
1 (0)	PCI33 Memory gap 1 enable 0 : disable 1 : enable, memory cycle which address fall in gap 1 will be passed to PCI
0 (0)	PCI33 Memory gap 0 enable 0 : disable 1 : enable, memory cycle which address fall in gap 0 will be passed to PCI

Note: For 98h Bit[1:0], they could not be set enable until the following condition is met:
1. memory mode register set (MRS) process has been done.
2. region of mgap is set (94h - 98h).

Register Index: Index 99h
Register Name: **Latch Control Signal Register H**
Attribute : Read/Write
Default Value 1Ah

Bit	Description
7:6	Reserve.
5:0	Ahead host clock stage to produce 100-133 or 100-166 pseudo bypass latch control signal. 1E : not ahead 1D : ahead 0.13x1 ns 1C : ahead 0.13x2 ns

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 9Ah
Register Name : **Latch Control Signal Register M**
Attribute : Read/Write
Default Value 17h

Bit	Description
7:6	Reserve
5:0	Ahead memory clock stage to produce 100-133 or 100-166 pseudo bypass latch control signal. 1E : not ahead 1D : ahead 0.13x1 ns 1C : ahead 0.13x2 ns

Register Index: Index 9Bh
Register Name: **Post Write Control Register**
Attribute : Read/Write

Bit	Description
7 (0)	Extra SMM gap enable 0 : disable 1 : enable, if memory cycle fall in extra smm gap , the behavior of this cycle is controlled by the setting of config. register of 93h bit[5:3]. NOTE : special smm gap is always 1M size, starting address is 1M below memory top.
6:3 (0000)	Reserve
2(0)	Shadow memory write enable lock bit 0 : disable, the shadow memory write enable bit and smm_access bit 93h[4] could be modified through normal configuration process. 1 : enable, the shadow memory write enable bit and smm_access bit would be read only. NOTE : this be could be programmed only during SMM routine period.
1(0)	Secondary bus (PCI66) memory gap 0 post write enable bit 0 : disable, any memory write cycle to PCI secondary bus would finish normally. 1 : enable, this bit is referenced when the R_POST_WT_EN(42hbit[3]) is enabled. And any memory write cycle to PCI secondary bus would response to cpu before write to bus.
0(0)	Secondary bus (PCI66) memory gap 1 post write enable bit 0 : disable, any memory write cycle to PCI primary bus would finish normally. 1 : enable, this bit is referenced when the R_POST_WT_EN(42hbit[3]) is enabled. And any memory write cycle to PCI secondary bus would be response to CPU before write to bus.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 9Ch
Register Name: **CPU Interface Control Register**
Attribute : [7:4] Reserve | [3:0] Read/Write

Bit	Description
7:6(00)	Reserve
5:4 (00)	On-chip CPU command queue depth selection 00 : depth is 1 01 : depth is 4 10 : depth is 8 11 : Reserve
3(0)	When primary PCI master and secondary PCI master issue cycles to DRAM at the same time, determine which one has higher priority to snoop CPU cache on CPU bus 0 : secondary PCI master has higher priority 1 : primary PCI master has higher priority
2(0)	Reserve
1(0)	Mask DBI_EN[3:0] to zero 0 : disable, DBI_EN drive by NB will pass to front side bus and data would invert timing 1 : enable, DBI_EN drive by NB will not pass and data keep the original one.
0 (0)	CPU interface of chip set will be able to perform burst read between consecutive H2M read cycles. When the bit is off, the data return of 2 H2M consecutive read cycles will have at least 1 turnaround cycle.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 9Dh
Register Name: **Host Clock and Memory Clock Frequency Detect**
Attribute : [7:3] Read only | [2:0] Read/Write

Bit	Description
7:6(00)	Host clock frequency, if real clocks relationship isn't one of the following, the value has no guarantee 00 : undetermined 01 : 2 X PCI clock 10 : 3 X PCI clock 11 : 4 X PCI clock Default : X
5:3(000)	Memory clock frequency, if real clocks relationship isn't one of the following, the value has no guarantee 000 : undetermined 001 : 2 X PCI clock 010 : 3 X PCI clock 011 : 4 X PCI clock 100 : 5 X PCI clock 101 : 6 X PCI clock Default : X
2:0 (110)	Frequency detection circuits determine the final result base on which number detections 000 : 1 time 001 : 2 times 010 : 3 times 011 : 4 times 100 : 5 times 101 : 6 times 110 : 7 times 111 : detect forever

Register Index: Index 9Eh
Register Name : **Host to Memory Read Enhance Control Register**
Attribute : [7:0] Read/Write

Bit	Description
7:6(00)	Reserve
5 (0)	CPU to memory read data path pseudo bypass enable bit. Only effective when pseudo bypass mode is enable. 0 : enable 1 : disable
4 (0)	Enhance host data dbi function timing. 0 : disable 1 : enable
3 (0)	Reserve.
2 (0)	H2M read half data mode. If it is enable, it will ahead drdy one cycle. But data strobe delay drdy half cycle. 0 : disable, h2m read data strobe synchronous with drdy. 1 : enable, h2m read data will return to CPU bus 1T faster than normal.
1 (0)	Ultra h2mr command bypass path enable. 0 : disable 1 : enable, the CPU to memory read command will pass to DRAM 2T faster than normal NOTE: this bit is valid only when RG_SPEC_ADS is enable.
0 (0)	Special h2mr command bypass path enable. 0 : disable 1 : enable, the CPU to memory read command will pass to DRAM 1T faster than normal

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index 9Fh
Attribute : [7:0] Read/Write

Bit	Description
7:0	Reserve

PCI PME Configuration Register

Register Index: Index A0h ~ A3h
Register Name: **Power Management Control Block #2 - Starting Address**
Attribute : Read/Write

Bit	Description
31:18 Undefined.	Reserve
17:16 (00)	00: M1671 will disable PM2_CNTL function. 01: Enable PM2CNTL function, but Read/Write this I/O port will transport to PCI bus. M1671 only monitor this byte setting and do the function. 10: Enable PM2CNTL function, but Read/Write this I/O port will not transport to PCI bus. 11: Reserve.
15:2 (11111111111111)	PM2_CNTRL Register.
1:0 (00b)	Reserve

Register Index: Index A4h
Register Name: **Power Management Capability Identifier Register**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah
Default Value 01h

Bit	Description
7:0	Capability Identifier. The capability identifier, when read by system software as 01h indicates that the data structure currently being pointed to is the PCI Power management data structure. The register default is read only, when index 4Ah bit 4 = 1, this register can read/write.

Register Index: Index A5h
Register Name: **Power Management Next Item Pointer Register**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah
Default Value 00h

Bit	Description
7:0	Next Item Pointer. This field provides an offset into the PCI configuration space pointing to the location of next item in the function capability list. If there is no additional item in the capability list, this register is set to 00h. The register default is read only, when index 4Ah bit 4 = 1, this register will be read/write.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index A6~A7h
Register Name: **Power Management Capabilities Register**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah

Bit	Description
15:11 (00000)	PME_Support XXXX1 : PMEJ and be asserted from D0 XXX1X : PMEJ and be asserted from D1 XX1XX : PMEJ and be asserted from D2 X1XXX : PMEJ and be asserted from D3 hot 1XXXX : PMEJ and be asserted from D3 cold These five bits field indicate the power state in which the function may assert PMEJ. A value of '0' for any bit indicates that the function is not capable of asserting the PMEJ signal while in that power state.
10 (0)	D2_Support 0 : Do not support D2 1 : Support D2 If this bit is set to '1', the M1671 supports the D2 power management state.
9 (0)	D1_Support 0 : Do not support D1 1 : Support D1 If this bit is set to '1', the M1671 supports the D1 power management state.
8:6 (000)	Reserve.
5 (0)	Device Specific Initialization (DSI) If this bit is set to '1', it indicates the function requires a device specific initialization sequence following transaction to the D0 un-initialized state.
4 (0)	Auxiliary Power Source. This bit is only meaningful if the bit 15 (PMEJ can be asserted from D3 cold) = 1 0 : Supply its own auxiliary power source 1 : Support PMEJ in D3 cold requires auxiliary power supplied by the system by way of proprietary delivery vehicle.
3 (0)	PME clock 0 : No PCI clock is required for M1671 to generate PMEJ. 1 : M1671 relies on the presence of the PCI clock for PMEJ operation.
2:0 (001)	Version of PCI power management interface specification. The version support is V1.0 now.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index A8~A9h
Register Name: **Power Management Control and Status Register**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah

Bit	Description
15 (0)	PME_Status (Read/Write_clear) This bit is set when the function would normal assert the PMEJ signal independent of the state of the PME_EN(index A8h bit 8) 0 : The function does not support PMEJ generation from D3 cold state. 1 : Indeterminate at time of initial OS boot if function supports PMEJ from D3 cold state. Write 1 to this bit will clear this bit to 0 and cause the M1647/M1671 to stop asserting a PMEJ(if enable). Writing a '0' has no effect.
14:13 (00)	Data_scale (Locked read/write) this two-bit field indicate the scaling factor to be used when interpreting the value of the DATA register (index ABh). The value & meaning of this field will vary depending on which data value has been selected bit[12-9] (DATA_select) field.
12:9 (0000)	Data_select (read/write) These four bits are used to select which data is to reported through DATA register (index ABh) and data scale (bit[14-13]) field.
8 (0)	PME_EN (read/write) 0 : PMEJ assertion is disable 1 : Enable the function to assert PMEJ
7:2 (000000)	Reserve (Locked read/write)
1:0 (00)	Power state (read/write) 00 : D0 01 : D1 10 : D2 11 : D3 hot These two bits are used to determine the current power state of a function and to set the function into a new power state. If software attempts to write an unsupported, optional state to this field. The write operation must complete normal on the bus, however the data is discarded and no state change occurs.

Register Index: Index AAh
Register Name: **PMCSR PCI to PCI bridge support extensions**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah

Bit	Description
7 (0)	Bus Power/Clock control enable 0 : Bus power/clock control mechanism has been disable 1 : Bus power/clock control mechanism has been enabled. When the bus Power/Clock control mechanism is disable, the bridge PMCSR Power State field cannot be used by the system software to control the power or clock of the bridge secondary bus.
6 (0)	B2/B3 support for D3 hot 0 : The bridge function is programmed to D3 hot, its secondary bus will have its power removed(B3) 1 : The bridge function is programmed to D3 hot, its secondary bus PCI clock will be stopped(B2) The state of this bit determines the action that is to occur as a direct result of programming the function to D3 hot. This bit is only meaningful if bit7 = 1(Bus Power/Clock control enable)
5:0 (000000)	Reserve

Register Index: Index ABh
Register Name: **Data Register**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah
Default Value 00h

Bit	Description
7:0	This register is used to report the state dependent data requested by the Data_Select (index A8h bit[12:9]) field. The value of this register is scaled by the value reported by the Data_Scale (index A8h bit[12:9]) field.

Register Index: Index AC ~ AFh
Register Name: Reserve

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HOST-to-PCI BRIDGE (Bus 0, Device 0)
AGP Interface Configuration Registers

Register Index: Index B0h-B3h
Register Name: **AGP Capability Identifier Register**
Attribute : Lock Read/Write by C8[12]

Bit	Description
31:24 (00h)	Reserve
23:20 (2h)	Major AGP Revision Number : The m1671 supports The Accelerated Graphics Port Interface Specification revision 2.0. So, this byte is contained of 2h.
19:16 (0h)	Minor AGP Revision Number: The m1671 supports The Accelerated Graphics Port Interface Specification revision 2.0. So, this byte is contained of 0h.
15:8(A4h)	Next Capability Pointer Number : The A.G.P. is the first capability of m1671. This pointer is hardwired to A4h to indicate the Second capability in list.
7:0 (02h)	AGP Capability ID : The value of 02h in this field identifies the list item as pertaining to A.G.P. registers.

Register Index: Index B4h-B7h
Register Name: **AGP Status Register**
Attribute : Lock Read/Write by C8[12]
Default Value 1B000217h

Bit	Description
31:24 (1Bh)	RQ : The M1671 supports the maximum number of AGP command request which is 1Bh.
23:10 (000000 00000000b)	Reserve
9 (1)	SBA : The M1671 supports the side band addressing. so the value of this bit is 1.
8:6 (000)	Reserve
5(0)	4G : if set, this device supports addresses greater than 4 GB.
4(1)	FW : When the bit is set, the device supports FW transfers.
3(0)	Reserve.
2:0 (111b)	Rate : The M1671 supports the 1x, 2x and 4x transfer rates, so the content of this byte should be 111b.

Register Index: Index B8h-BBh
Register Name: **A.G.P. Command Register**
Attribute : Read/Write
Default Value 00000000h

Bit	Description
31:24	Reserve
23:10	Reserve
9	When set, the side band address mechanism is enabled in the m1671.
8	This bit allows the master to initiate A.G.P. operations. When cleared, the master cannot initiate A.G.P. operation.
7:6	Reserve
5	4G : Setting the 4G bit allows the master to initiate A.G.P Requests to accept A.G.P protocol DAC commands when bit 9 is cleared. Setting the 4G bit enables the target to accept a Type 4 command and to utilize A[35::32] for a Type 3 command when bit 9 is set.
4	FW_Enable : When this bit is set, the device must do Memory Write transactions from the core-logic to the A.G.P master following FW protocol. When this bit is cleared memory write transactions from the core-logic to the A.G.P master follow standard PCI protocol.
3	Reserve
2:0	Data_Rate : One and only one bit in this field must be set to indicate the desired data transfer rate. bit 0 1x bit 1 2x bit 2 4x

HOST-to-PCI BRIDGE (Bus 0, Device 0)
A.G.P. GART/GTLB Configuration Registers

Register Index: Index BCh~BFh
Register Name: **GART Base Address and NLVM Size**
Attribute : Read/Write
Default : 00000000h

Bit	Description
31:12	Define the bass address (4k based) of the GART allocated in the system memory.
11:4	Reserve
3:0	Define the size of the NLVM. '0000' : 0 MB '0001' : 1 MB '0010' : 2 MB '0011' : 4 MB '0100' : 8 MB '0101' : Reserve '0110' : 16 MB '0111' : 32 MB '1000' : 64 MB '1001' : 128 MB '1010' : 256 MB others : Reserve

Register Index: Index C0h~C3h
Register Name: **Level2 GTLB Control**
Attribute : Read/Write
Default : 10130000h

Bit	Description
31:28	WBUF GTLB Snoop latency
27:24	MSEQ Level 0 GTLB Snoop Latency
23:20	WBUF GTLB Snoop Slice
19:16	MSEQ Level0 GTLB Snoop Slice
15:14	Reserve
13:12	Master High Priority Check [13]: Master1 High Priority Check '0': Check '1': Never Check [12]: Master0 High Priority Check '0': Check '1': Never Check
9:8	Arbitration Mode "00" : MSEQ level0 GTLB snoop -> WBUF GTLB snoop others : WBUF GTLB snoop -> MSEQ level-0 GTLB snoop
7:6	Reserve
5:4	GTLB Size Setting 00 : 128 entries 01 : 64 entries 10 : 32 entries 11 : 16 entries
3:0	Reserve

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index C4h~C7h
Register Name: **GTLB Control**
Attribute : Read/Write
Default : 00h

Bit	Description
31:15	TAG address to be invalidate when C4[0] be set.
14:2	Reserve.
1	If set to '1', all the GTLB will be invalidated when C4[0] is set to '1'. '0' : Disable '1' : Enable
0	When set to '1', the GTLB TAG specified by C4[31:15] will be invalidated. If C4[1] is '1', all the GTLB TAG will be invalidated. After the invalidating process be completed, this bit will be clear to '0' automatically. '0' : Disable '1' : Enable

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index C8h~CBh
Register Name: **AGP Control Register Two**
Attribute : Read/Write

Bit	Description
31 (1)	AGP read command order enhance mode 0 : safe mode
30 (1)	AGP write command order enhance mode 0 : safe mode
29 (0)	Low priority read and write slice timer enable bit. Set to 0 for normal operation.
28 (0)	Low priority read latency counter enable bit. Set to 0 for normal operation.
27:24 (0000)	Low priority read and write slice timer
23:16 (00000000)	Low priority read latency counter
15 (0)	Internal debug mode (set to 0 for normal operation)
14 (1)	8QW length command enhance mode 0 : 4QW command mode 1 : 8QW command mode
13 (1)	Internal debug mode. Set to 1 for normal operation.
12 (0)	AGP STATUS lock read/write bit. 0 : Disable -- AGP STATUS and Identifier register is read only 1 : Enable -- AGP STATUS and Identifier register is read/write
11 (1)	Internal debug mode (set to 1 for normal operation)
10:8(000)	Internal debug mode (set to '000' for normal operation)
7 (1)	AGP read data buffer depth. 0 : 16QW(32QW) 1 : 32QW(64QW)
6:4 (000)	Reserve
3 (0-gated)	AGP MCLK domain gated disable; when D0[4]='1' and this bit set to 0, the internal buffers of MCLK domain will be gated.
2 (0-gated)	AGP GCLK domain gated disable; when D0[4]='1' and this bit set to 0, the internal buffers of GCLK domain will be gated.
1 (0-gated)	AGP controller gated disable; when D0[4]='1' and this bit set to 0, the AGP control circuit will be gated.
0 (0-gated)	AGP configuration gated disable; when D0[4]='1' and this bit set to 0, the AGP configuration registers and control circuit will be gated.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index CCh~CFh
Register Name: **GTLB TAG Status**
Attribute : Read/Write
Default : 00000000h

Bit	Description
31:15	Data of GTLB TAG selected by CC[3:0]. This is chipset internal debugging option. Attribute : Read Only
14:9	Reserve.
8	Status of GTLB TAG selected by CC[3:0]. This is chipset internal debugging option. Attribute : Read Only
7:4	Reserve
3:0	GTLB TAG select. This is chipset internal debugging option. 0000 : TAG0 0001 : TAG1 0010 : TAG2 . 1111 : TAG15

Clock/Timing Control Configuration Registers

Register Index: Index D0h
Register Name: **Global Gated Clock Control**
Attribute Read/Write

Bit	Description
7 (0)	Host Interface Gated Clock 0 : disable 1 : enable
6 (0)	DRAM self-refresh option when SUSPEND# is asserted. This configuration is used for the SMA mode. 0 : DRAM enters self-refresh. 1 : Keep DRAM in normal operation mode.
5 (0)	PCI Interface Gated Clock 0 : disable 1 : enable
4 (0)	AGP Interface Gated Clock 0 : disable 1 : enable
3 (0)	Memory Interface Gated Clock 0 : disable 1 : enable
2 (0)	PLL power down during STR (Suspend To RAM)/StopCLK 0 : disable 1 : enable
1:0 (00)	PLL power-down exit lock time 00 : 1 ms 01 : 128 us 10 : 64 us 11 : 32 us

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index D1h
Register Name: **Memory Interface Timing Compensation Control I**
Attribute : Read/Write
Default : F0h

Bit	Description
7:4	SDR write clock timing ahead offset (15 stages, 0.28ns/stage) 1111: 0 stages 1110: 1 stage 1101: 2 stages 1100: 3 stages 1011: 4 stages 1010: 5 stages 1001: 6 stages 1000: 7 stages 0111: 8 stages 0110: 9 stages 0101: 10 stages 0100: 11 stages 0011: 12 stages 0010: 13 stages 0001: 14 stages 0000: 15 stages
3:2	DDR-SDRAM read input enable reset timing compensate (4 stages, 0.2ns/stage) Internal debugging purpose only. Set to 00 for normal operation.
1:0	DDR-SDRAM read input enable set timing compensate (4 stages, 0.2ns/stage) Internal debugging purpose only. Set to 00 for normal operation.

Register Index: Index D3-D2h
Register Name **Memory Interface Timing Compensation Control II**
Attribute : Read/Write
Default : FF5Ch

Bit	Description
15:12	MA/SRAS/SCAS/MWE output timing ahead offset (15 stages, 0.28ns/stage) 1111: 0 stages 1110: 1 stage 1101: 2 stages 1100: 3 stages 1011: 4 stages 1010: 5 stages 1001: 6 stages 1000: 7 stages 0111: 8 stages 0110: 9 stages 0101: 10 stages 0100: 11 stages 0011: 12 stages 0010: 13 stages 0001: 14 stages 0000: 15 stages
11:8	CS[5:0]/CKE[5:0] output timing ahead offset (15 stages, 0.28ns/stage) 1111: 0 stages 1110: 1 stage 1101: 2 stages 1100: 3 stages 1011: 4 stages 1010: 5 stages 1001: 6 stages 1000: 7 stages 0111: 8 stages 0110: 9 stages 0101: 10 stages 0100: 11 stages 0011: 12 stages 0010: 13 stages 0001: 14 stages 0000: 15 stages
7:4	MD input Timing delay offset (15 stages, 0.28ns/stage) 1111: 15 stages 1110: 14 stages 1101: 13 stages 1100: 12 stages 1011: 11 stages 1010: 10 stages 1001: 9 stages 1000: 8 stages 0111: 7 stages 0110: 6 stages 0101: 5 stages 0100: 4 stages 0011: 3 stages 0010: 2 stages 0001: 1 stage 0000: 0 stages
3:0	MCLK domain global timing offset (15 stages, 0.14ns/stage) Internal debugging purpose only, set 0xC for normal operation

Register Index: Index D7-D4h
Register Name: **DDR DQ/DQS clock source ahead compensation** => Attribute: [28:24] Read/Locked-Write
Memory Interface I/O driver control => Attribute : [23:10] Read/Write,
Memory Interface DLL/process-monitor status report register => Attribute : [8:0] Read-Only
Default : 1A555000h

Bit	Description
31:29	Reserve
28:24	DDR SDRAM DQ/DQS clock source ahead compensation (31 stages,0.14ns/stage) 11111: 0 stages 11110: 1 stage : : 00001: 30 stages 00000: 31 stages
23:20	MD Driving Strength Unit:mA 0x1 3.7 0x2,4 7.4 0x3,5,8 11.2 0x6,9 14.9 0x7,A,C 18.6 0xB,D 22.4 0xE 26.1 0xF 29.8
19:16	CSJ/CKE Driving Strength Unit:mA 0x1 3.7 0x2,4 7.4 0x3,5,8 11.2 0x6,9 14.9 0x7,A,C 18.6 0xB,D 22.4 0xE 26.1 0xF 29.8
15:12	MA/SRAS/SCAS/MWE Driving Strength Unit:mA 0x1 7.6 0x2,4 11.5 0x8 15.3 0x3,5 19.2 0x6,9 23.0 0xA,C 27.0 0x7 30.0 0xB,D 34.5 0xE 38.3 0xF 46.0
11:9	Reserve
8(RO)	DDLL clock period info sample out
7:0(RO)	Effective delay stages used in DDR/SDR compensation.

Register Index: Index D8h
Register Name: **NB CPU Interface PLL Reserved Register**
Attribute : Read/Write

Bit	Description
7:0 (00h)	Reserved for CPU interface side PLL usage Internal debugging purpose only. Set to 00h for normal operation.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index D9h
Register Name: **NB CPU_Interface PLL Control Register**

Bit	Description
7 (0)	PLL Charge Pump Control circuit Enable Attribute : Read/Write/Hardware Setting 0 : disable 1 : enable
6:5 (10)	PLL Charge Pump Current Control Enable Attribute : bit[1] Read/Write/Hardware Setting Attribute : bit[0] Read/Write 00 : 10uA 01 : 20uA 10 : 30uA 11 : 40uA
4:3 (00)	PLL Damping Factor Register Control Attribute : Read/Write 00 : 4K 01 : 8K 10 : 12K 11 : 16K
2:1 (00)	PLL Vco Max Frequency control Attribute : Read/Write 00 : 550 MHz 01 : 575 MHz 10 : 600 MHz 11 : 625 MHz
0 (0)	PLL Ext/Int Loop Setting Attribute : Read/Write 0 : external 1 : internal

Register Index: Index DAh
Register Name: **HOST Data Output 400MHz Clock Delay Line Delay**
Attribute Read/Write
Default Value : 1Ah

Bit	Description
7:5 (000)	Reserve
4:0 (11010)	HOST Data output 400MHz clock delay line delay selection, one unit is 0.14 ns.

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index DBh
Register Name : **NB Frequency Interface Control Register**

Bit	Description
7 (0)	1 level fully-asynchronous 0 : 2 level flip-flop 1 : 1 level flip-flop
6 (0)	Host and memory interface same frequency bypass mode interface under same frequency 0 : Disable, fully-asynchronous 1 : Enable. Bypass the Frequency-Interface
5 (0)	Host to PCI interface enhance-mode 0 : Disable, fully-asynchronous 1 : Enable. Enable the enhance mode
4 (0)	Host and memory interface 100-133MHz async bypass mode 0 : Disable, fully-asynchronous 1 : Enable. Enable the enhance mode
3(0)	Host and memory interface 100-166MHz async bypass mode 0 : Disable, fully-asynchronous 1 : Enable. Enable the enhance mode
2 (0)	Host and memory interface force same frequency bypass mode 0 : Disable, fully-asynchronous 1 : Enable. Enable the enhance mode
1(0)	Host and memory interface force 100-133MHz async bypass mode 0 : Disable, fully-asynchronous 1 : Enable. Enable the enhance mode
0(0)	Host and memory interface force 100-166MHz async bypass mode 0 : Disable, fully-asynchronous 1 : Enable. Enable the enhance mode

Register Index: Index DCh
Register Name: **NB Host PLL Control Register**

Bit	**Description**
7(1)	Host PLL Enable 0 : Disable 1 : Enable
6:4(000)	Reserve
3(0)	HPLL compensation direction control 0 : delay to external clock 1 : ahead of external clock
2:0 (000)	HPLL Delay Selection

Register Index: Index DDh
Register Name: **NB Memory PLL Control Register**

Bit	Description
7 (1)	Memory PLL Enable 0 : Disable 1 : Enable
6:4 (000)	Reserve
3(0)	MPLL compensation direction control 0 : delay to external clock 1 : ahead of external clock
2:0 (000)	MPLL Delay Selection

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index DEh
Register Name: **NB AGP PLL Control Register**

Bit	Description
7 (1)	AGP PLL Enable 0 : Disable 1 : Enable
6:4(000)	Reserve
3(0)	GPLL compensation direction control 0 : delay to external clock 1 : ahead of external clock
2:0 (000)	GPLL Delay Selection

Register Index Index DFh
Register Name: **Other NB PLL Control Register**

Bit	Description
7:0	Other NB PLL Control Register

Register Index: Index E3-E0h
Register Name: **Memory Interface DDR-SDRAM DDLL 1/4 T Delay Generator Control**
Attribute : Read/Write

Bit	Description
31 (0)	DDLL fundamental operation mode 0 : Hardware mode(power-up init sequence required, see Bit[8] below) 1 : Software mode
30 (0)	DDLL locking reference period. 0 : Full clock period 1 : Half clock period
29:24 (111010)	DDLL output reference delay offset factor for read path (OFFST) Note1: this is a signed integer, range from -31 to +31 Note2: The effective delay value(EFFD) used for 1/4T locking is EFFD=DDLL_OUT/4 + OFFSET where DDLL_OUT=reference delay value of 1 clock period recognized by DDLL
23:16(0)	Reserve
15:9 0110000(48d)	DDLL software-mode delay stages control(128 stages)
8 (0)	DDLL/process-monitor power-up initialization. Enable this bit for at least 5 us to make DDLL/process-monitor stable before any DDR SDRAM read/write accesses. Note: always disable this bit for DDLL software mode. 0 : disable (normal operation for DDLL hardware mode) 1 : enable
7 (0)	DDLL/process-monitor status read data output control 0 : disable(always report 0 to avoid ambiguous) 1 : enable
6:0(0000000)	Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index E7-E4h
Register Name: **Memory Interface DDR SDRAM Output(write)-Path DLL Configuration**
Attribute : Read/Write

Bit	Description
31:30 (01)	DQS_CLK compensation mode 00 : Reserve 01 : digital-dll(DDLL) auto mode (derived from inversed & delayed MCLK) 10 : digital-dll(DDLL) software mode 0 (derived from delayed MCLK) 11 : digital-dll(DDLL) software mode 1 (derived from inversed & delayed MCLK)
29:24(000000)	DQS_CLK delay/offset control: (depends on the DQS_CLK compensation mode specified.) When DDLL auto mode:(signed integer, range from -31 to +31). Value is used to offset the DQS_CLK ahead/delay level relative to core MCLK. bi-directional, ahead or delay. When DDLL software mode: (unsigned integer, range from 0 to 63). Value is used to offset the DQS_CLK delay level relative to core MCLK. Single-directional, delay only. default : 101111 (-17d) for DDLL auto mode(for compensating delay of 4*muxi2x2 + 1*mxi2x4 + o_pad)
23 (1)	DQ_CLK compensation mode 0 : Reserve 1 : digital-dll(DDLL)/software mode
22 (0)	Reserve.
21:16 (000000)	DQ_CLK delay/offset control: (depends on DQ_CLK compensation mode specified) When DDLL mode: (signed integer, range from -31 to +31). Value is used to offset the DQ_CLK 1/4 T delay level relative to DQS_CLK. bi-directional, ahead or delay.
15:0(0000h)	Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)
AGP DLL and I/O PAD Configuration Registers

Register Index: Index E8-EBh
Register Name: **AGP DLL Control Register**
Attribute : Read/Write

Bit	Description
31:24(00000000)	AGP DLL stage selection (read only)
23:22(00)	Reserve
21 (0)	AGP DLL stage auto detection enable
20(0)	AGP DLL lead/lag status register (read only)
19:16 (8h)	The multiply number (will be divided by 32) of AGP DLL stage
15 (0)	AGP DLL stage number read enable
14 (0)	AGP DLL lock half clock instead of full clock for low frequency issue
13:8 (000000)	The offset number of AGP DLL stage
7 (0)	Enable the software control (configuration) of AGP DLL stage
6(0)	Reserve
5:0 (20h)	The stage number of AGP DLL

Register Index: Index EC-EFh
Register Name: **AGP I/O Pad Tracking Circuit Control**
Attribute : Read/Write

Bit	Description
31:16(0000h)	Reserve
15:14(00)	Reserve
13:8(0)	Read Only, tracking data from the track ckt P1X,P2X,P4X,N1XN,N2XN,N4XN
7 (0)	Tracking data write enable. --RG_TRACK_WEN AGP I/O Pad driving will be selected from the software programmed data (configuration) instead of from the tracking circuit when this bit is set.
6(0)	Reserve.
5:0 (000000b)	AGP I/O Pad driving selected bits P1X,P2X,P4X,N1XN,N2XN,N4XN

Spare Configuration Register

Register Index: Index F0h
Register Name: **CPU STB_IN Delay Selection Register**
Attribute : Read/write for Bit[3:0]

Bit	Description
7:4(0h)	Reserve
3:0(0h)	Delay stage selection for CPU write data strobe (DSTBp/DSTBn) compared with related data bus 1 stage : 15ns

Register Index: Index F1h
Register Name: **CPU IO DLL Status Register**
Attribute : Read only for Bit[7], Reserve for Bit[6:0]

Bit	Description
7 (0)	Process Monitor Status 0 : invalid 1 : valid
6:0 (0000000)	Reserve

HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index F2h
Register Name: **CPU DLL Soft Mode Register**
Attribute : Read/Write

Bit	Description
7(0)	Process Monitor software mode enable 0 : disable 1 : enable
6:0 (0000000)	Process Monitor software mode selection

Register Index: Index F3h
Register Name: **CPU DLL Status Register**
Attribute : Read only
Default Value 00h

Bit	Description
7:0	Process monitor sampled value.

Register Index: Index F4~F5h
Register Name: **NB ADDR/DATA STBPJ/STBNJ Delay Line Control**
Attribute : Read / HW SETTING

Bit	Description
15:12	Delay stage selection of CPU read data strobe compared with related data bus default : HW SETTING 1.F4h[3]= 1 : when '0000' => 0 stage when '0001' => 1 stage; 1stage=0.15ns when '0010' => 2 stages when '0011' => 3 stages when '0100' => 4 stages when '0101' => 5 stages when '0110' => 6 stages when '0111' => 7 stages when '1000' => 8 stages when '1001' => 9 stages when '1010' => 10 stages when '1011' => 11 stages when '1100' => 12 stages when '1101' => 13 stages when '1110' => 14 stages when '1111' => 15 stages 2.F4h[3]= 0 : when '0000' => 1/64 T, T=1CPU front side bus cycle time when '0001' => 2/64 T when '0010' => 3/64 T when '0011' => 4/64 T when '0100' => 5/64 T when '0101' => 6/64 T when '0110' => 7/64 T when '0111' => 8/64 T when '1000' => 9/64 T when '1001' => 10/64 T when '1010' => 11/64 T when '1011' => 12/64 T when '1100' => 13/64 T when '1101' => 14/64 T when '1110' => 15/64 T when '1111' => 16/64 T

11:8	Delay selection of CPU read data strobe (DSTBNJ) compared with related data bus. default : HW SETTING 1.0xF4[3] = 1 : when '0000' => 0 Stage when '0001' => 1 Stage, 1 stage=0.15ns when '0010' => 2 Stages when '0011' => 3 Stages when '0100' => 4 Stages when '0101' => 5 Stages when '0110' => 6 Stages when '0111' => 7 Stages when '1000' => 8 Stages when '1001' => 9 Stages when '1010' => 10 Stages when '1011' => 11 Stages when '1100' => 12 Stages when '1101' => 13 Stages when '1110' => 14 Stages when '1111' => 15 Stages 2.F4hbit[3] = 0: when '0000' => 1/64 T, T=1CPU front side bus cycle time when '0001' => 2/64 T when '0010' => 3/64 T when '0011' => 4/64 T when '0100' => 5/64 T when '0101' => 6/64 T when '0110' => 7/64 T when '0111' => 8/64 T when '1000' => 9/64 T when '1001' => 10/64 T when '1010' => 11/64 T when '1011' => 12/64 T when '1100' => 13/64 T when '1101' => 14/64 T when '1110' => 15/64 T when '1111' => 16/64 T
7:4	Delay selection of M1671 issued master cycle command strobe (ADSTBJ) compared with related address bus default : HW SETTING 1.F4h bit[3] = 1 : when '0000' => 0 Stage when '0001' => 1 Stage, 1stage=0.15 ns when '0010' => 2 Stages when '0011' => 3 Stages when '0100' => 4 Stages when '0101' => 5 Stages when '0110' => 6 Stages when '0111' => 7 Stages when '1000' => 8 Stages when '1001' => 9 Stages when '1010' => 10 Stages when '1011' => 11 Stages when '1100' => 12 Stages when '1101' => 13 Stages when '1110' => 14 Stages when '1111' => 15 Stages 2.F4h bit[3] = 0 : when '0000' => 1/32 T, T=1CPU front side bus cycle time when '0001' => 2/32 T when '0010' => 3/32 T

	when '0011' => 4/32 T when '0100' => 5/32 T when '0101' => 6/32 T when '0110' => 7/32 T when '0111' => 8/32 T when '1000' => 9/32 T when '1001' => 10/32 T when '1010' => 11/32 T when '1011' => 12/32 T when '1100' => 13/32 T when '1101' => 14/32 T when '1110' => 15/32 T when '1111' => 16/32 T Note: The delay selection is determined by hardwire setting during reset period.
3 (0)	the delay selection of 0xF4h[5:4]~F5h[7:0]. 0 : disable 1 : enable, this will be determined by CLK_STAGE and multi-value.
2 (0)	the DELAY selection will run time update if enable. Attribute : Read / Write 0 : disable 1 : enable
1:0(00)	Strobe delay selection output control Attribute : Read / Write 00 : disable 01 : from adstbj block 10 : from dstbnj block 11 : from dstbpj block

Register Index: Index F6h
Register Name: **NB CPU_INFX_DLL_COMP_OUT**
Attribute : Read Only
Default Value : 00h

Bit	Description
7:0	Delay stages of command/data strobe The stages of DLL_Multi_Mode calculated result when DLL_OUTPUT_EN_SEL : 00 : 00h when DLL_OUTPUT_EN_SEL : 01 : latch from adstbj block when DLL_OUTPUT_EN_SEL : 10 : latch from dstbnj block when DLL_OUTPUT_EN_SEL : 11 : latch from dstbpj block Note: This value is valid only when F4hbit[3] is 0.

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HOST-to-PCI BRIDGE (Bus 0, Device 0)

Register Index: Index F7h
Register Name: Reserve
Default : 00h

Register Index: Index F8~F9h
Register Name: **Configuration Registers Reserved for BIOS use**
Attribute : Read/Lock Write, control bit is x4Ah bit4.
Default Value: 0000h

Register Index: Index FAh
Register Name: **Real Revision ID and Revision ID.**
Attribute : Read/Lock Write, control bit is x4Ah bit4.
Default Value 01h

Bit	**Description**
31:24	Real Device ID.

Register Index: Index FBh
Register Name: **Real Device ID and Revision ID.**
Attribute : Read/Lock Write, control bit is x4Ah bit4.
Default Value 47h

Bit	Description
23:16	Real Revision ID.

Register Index: Index FC~FFh
Register Name: **Configuration Registers Reserved for BIOS use**
Attribute : Read/Write
Default Value : 0000h

PCI-to-PCI BRIDGE -- Bus 0, Device 1

Index	Name	Attribute	Def.Value
00h-01h	Vender Identification Register	R	10B9h
02h-03h	Device Identification Register	R/W lock	5247h
04h-05h	Command Register	R/W	0000h
07h-06h	Status Register	R/W	0000h
08h	Revision Identification Register	R	01h
09h	Specific Register-Level Programming Register	R	00h
0Ah	Sub-Class Code Register	R	04h
0Bh	Base-Class Code Identification Register	R	06h
0Eh	Header Type Register	R	01h
0Fh-17h	Reserve		
18h	Primary Bus Number Register	R	00h
19h	Secondary Bus Number Register	R/W	00h
1Ah	Subordinate Bus Number Register	R/W	00h
1Bh	Reserve		
1Ch	IO Base Address Register	R/W	F0h
1Dh	IO Limit Address Register	R/W	00h
1Eh-1Fh	Secondary PCI-PCI Status Register	R/W	0020h
20h-21h	Memory Base Address Register	R/W	FFF0h
22h-23h	Memory Limit Address Register	R/W	0000h
24h-25h	Prefetchable Memory Base Address Register	R/W	FFF0h
26h-27h	Prefetchable Memory Limit Address Register	R/W	0000h
28h-3Dh	Reserve		
3Eh-3Fh	PCI-to-PCI Bridge Control Register	R/W	0000h

PCI-to-PCI BRIDGE -- Bus 0, Device 1

Register Index: Index 00h-01h
Register Name: **Vender Identification Register**
Attribute : Read
Default : 10B9h

Bit	Description
15:0	This is a 16-bit value assigned to Acer Laboratories Inc.

Register Index: Index 02-03h
Register Name: **Device Identification Register**
Attribute : Read/ Lock Write controlled by Bit4 of Index 4Ah
Default : 5247h

Bit	Description
15:0	This is a 16-bit value assigned to P2P bridge of ALI's M1671.

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PCI-to-PCI BRIDGE -- Bus 0, Device 1

Register Index: Index 04-05h
Register Name: **Command Register**
Attribute : Read/Write

Bit	Description
15:9(0000000)	Reserve.
8 (0)	SERR# Enable : This bit is an enable bit for the SERR# driver. When this bit is set, the M1671 SERR# signal driver is enabled for the error condition that occurred on the A.G.P. bus.
7 (0)	Reserve.
6 (0)	Parity Error Response: When the bit is set, M1671 will take its normal action when a parity error is detected. When the bit is 0, the M1671 will ignore any parity errors that it detects and continue normal operation.
5:2 (0h)	Reserve.
1 (0)	Memory Space Enable : control P2P's response to memory space accesses on primary bus. A value of 0 disables the P2P response. A value of 1 allows the device to respond to memory space access.
0 (0)	I/O Space Enable : control P2P's response to I/O space accesses on primary bus. A value of 0 disables the P2P response. A value of 1 allows the device to respond to I/O space access.

Register Index: Index 07-06h
Register Name: **Status Register**
Attribute : Read/Write

Bit	Description
15 (0)	Reserve
14 (0)	When the M1671 asserts the SERR# due to error conditions on the A.G.P. bus. This bit will be set to 1.
13:0 (0000000 0000000)	Reserve

Register Index: Index 08h
Register Name: **Revision Identification Register**
Attribute : Read
Default Value 01h

Bit	Description
7:0	This is an 8-bit value that indicates the revision identification number for P2P bridge of M1671.

PCI-to-PCI BRIDGE -- Bus 0, Device 1

Register Index: Index 09h
Register Name: **Specific Register-Level Programming Register**
Attribute : Read
Default Value 00h

Bit	Description
7:0	This value of P2P bridge in M1671 is 00h.

Register Index: Index 0Ah
Register Name: **Sub-Class Code Register**
Attribute : Read
Default Value 04h

Bit	Description
7:0	This value of P2P bridge is 04h.

Register Index: Index 0Bh
Register Name: **Base-Class Code Identification Register**
Attribute : Read
Default Value 06h

Bit	Description
7:0	This value of P2P bridge in M1671 is 06h.

Register Index: Index 0Eh
Register Name: **Header Type Register**
Attribute : Read
Default Value 01h

Bit	Description
7:0	This Header Type value of P2P bridge in M1671 is 01h.

Register Index: Index 18h
Register Name: **Primary Bus Number Register**
Attribute : Read
Default Value 00h

Bit	Description
7:0	The primary bus number of host bridge should be 00h

Register Index: Index 19h
Register Name: **Secondary Bus Number Register**
Attribute : Read/Write
Default Value 00h

Bit	Description
7:0	This register identifies the bus number assigned to the second bus side -- A.G.P. bus of the P2P bridge in M1671.

Register Index: Index 1Ah
Register Name: **Subordinate Bus Number Register**
Attribute : Read/Write
Default Value 00h

Bit	Description
7:0	This register identifies the subordinate bus number assigned to the second bus side – A.G.P. bus of the P2P bridge in M1671.

PCI-to-PCI BRIDGE -- Bus 0, Device 1

Register Index: Index 1Ch
Register Name: **IO Base Address Register**
Attribute : Read/Write

Bit	Description
7:4 (Fh)	These four bits correspond to A[15:12] of the I/O address.
3:0 (0h)	Reserve

Register Index: Index 1Dh
Register Name: **IO Limit Address Register**
Attribute : Read/Write

Bit	Description
7:4(0h)	These four bits correspond to A[15:12] of the I/O address
3:0(0h)	Reserve

Register Index: Index 1E-1Fh
Register Name: **Secondary PCI-PCI Status Register**
Attribute : Read/Write

Bit	Description
15 (0)	Detected Parity Error on A.G.P. bus: The M1671 will set this bit whenever it detects a parity error, even if parity error handling is disabled.
14(0)	Received SERR# on A.G.P. bus: The M1671 will set this bit when it detects GSERR# assertion on A.G.P. bus.
13 (0)	Received Master Abort on A.G.P. bus: The M1671 will set this bit when its Secondary PCI transaction is terminated with Master-Abort.
12(0)	Received Target Abort on A.G.P. bus: The M1671 will set this bit when its Secondary PCI transaction is terminated with Target-Abort.
11:9	Reserve
8 (0)	Data Parity Error Detected on A.G.P. bus side: This bit will be set to 1, when three condition are meet: 1. The M1671 asserted GPERR# or sampled GPERR# asserted.2. The M1671 was the initiator for the operation in which the parity error occurred.3. The bit 0 is 1 in CR_PPBCR -- bridge control register.
7:0(20h)	Reserve

Register Index: Index 20-21h
Register Name: **Memory Base Address Register**
Attribute : Read/Write

Bit	Description
15:4 (FFFh)	These twelve bits correspond to A[31:20] of the Memory address
3:0(0h)	Reserve

Register Index: Index 22-23h
Register Name: **Memory Limit Address Register**
Attribute : Read/Write

Bit	Description
15:4(000h)	These twelve bits correspond to A[31:20] of the Memory address
3:0(0h)	Reserve

Register Index: Index 24-25h
Register Name: **Prefetchable Memory Base Address Register**
Attribute : Read/Write

Bit	Description
15:4(FFFh)	These twelve bits correspond to A[31:20] of the Memory address
3:0(0h)	Reserve

PCI-to-PCI BRIDGE -- Bus 0, Device 1

Register Index: Index 26-27h
Register Name: **Prefetchable Memory Limit Address Register**
Attribute : Read/Write

Bit	Description
15:4(000h)	These twelve bits correspond to A[31:20] of the Memory address
3:0(0h)	Reserve

Register Index: Index 3E-3Fh
Register Name: **PCI-PCI Bridge Control Register**
Attribute : Read/Write

Bit	Description
15:4(000h)	Reserve
3(0)	VGA Enable : When this bit is set, the M1671 will positively decode and forward the following accesses to A.G.P. bus. Memory accesses in the range 0A0000h to 0BFFFFh I/O accesses where AD Bit [9:0] are in the ranges 3B0h-3B9h, 3C0h-3DFh.
2(0)	ISA Enable: When this bit is set, the M1671 will block any forwarding to A.G.P. bus of I/O transaction addressing the last 768 bytes in each 1k byte block. And M1671 will transfer those I/O transactions to primary PCI bus.
1(0)	System Error Enable: When this bit is set and the GSERR# enable bit in command register is set, the M1671 will forward GSERR# assertions to the primary bus -- SERR#.
0(0)	Parity Error Response Enable: When this bit is 0, the M1671 will ignore data parity error on the A.G.P. bus. Otherwise, the M1671 will assert GPERR# when it detects the data parity errors on the A.G.P. bus.

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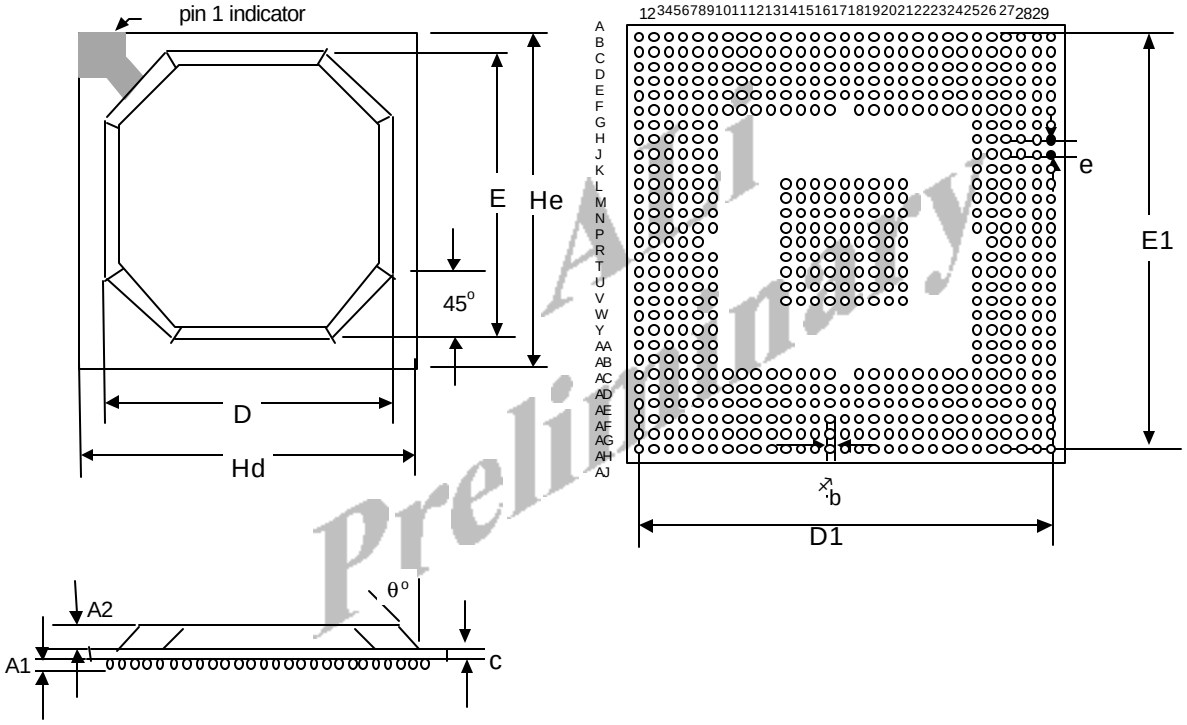
Section 7 : Packaging Information

BGA Dimension Specification (37.5mm x 37.5mm)
629 BGA



Symbol	Min.	Nom.	Max.
A1	0.55	0.60	0.65
A2	1.12	1.17	1.22
ϕ b	0.60	0.75	0.90
c	0.51	0.56	0.61
D	34.30	34.50	34.70
D1	35.36	35.56	35.76
E	34.30	34.50	34.70
E1	35.36	35.56	35.76
e		1.27	
Hd	37.30	37.50	37.70
He	37.30	37.50	37.70
θ °	23°	30°	37°
Y(ball diameter)			0.75

Section 8 : Revision History

Initial version 0.30 (printout)

Ver.0.40	DDR pinout diagram(pp.12-15), p.79,97,99,100,103,104	09/14/2001
Ver.0.50	Pins AGPGND, P1A to NC, major cleanup	10/14/2001
Ver.0.60	Hardware Setup Table revised,p.42,56,62,64,66,67	11/14/2001

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