

The production release of the Microcode Update for the Slot 1 Deschutes and Covington processors dA0 stepping is now available from Intel. Intel requires the appropriate Microcode Update to be loaded into all Pentium® Pro and Pentium II family processors as Intel processors are only validated with the appropriate Microcode Update applied.

This Microcode Update contains workarounds for Errata #37 and #38 in the January NDA Pentium II Processor Specification Update. On the Covington processor, the Microcode Update initializes the processor for optimum L2 cacheless operations.

MU165027.txt contains the assembly code version of the Microcode Update for the Slot 1 Deschutes and Covington dA0 production processors. S1\_8.pdb contains Microcode Updates for Slot 1 Deschutes and Covington dA0 stepping, the Pentium II Processor C0 and C1 stepping. S1\_8.pdb is intended for use with the "checkup1.exe" utility.

Starting with Deschutes processors, the naming convention adapted for \*.txt microcode Update files is as follows:

MUABCDEF.txt, where:

MU = Microcode Update

A = "A" is 1 for Slot 1 and 2 for Slot 2

B = "B" reflects the model as reported by CPUID instruction

C = "C" reflects the family as reported by CPUID instruction

D = "D" reflects the stepping as reported by CPUID instruction

EF = "EF" reflects the revision no. of Microcode Update within a stepping, for more information, please see chapter 8 of "Pentium(r) Pro Processor BIOS Writer's Guide"