AMD Athlon™ XP Processor Model 10 with 256K L2 Cache Data Sheet

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Trademarks

Contents

List of Figures

List of Tables

Revision History

Date	Rev	Description
April 2004	C	Added Table 2, "Electrical and Thermal Specifications for the AMD Athlon™ XP Processor Model 10 with 256K L2 Cache with VCC_CORE = 1.50 V," on page 3, and updated Table 3, "OPN of the AMD Athlon™ XP Processor Model 10 with 256K L2 Cache," on page 9.
September 2003	B	First public release of the *AMD Athlon™ XP Processor Model 10 with 256K L2 Cache Data Sheet*

AMD Athlon™ XP Processor Model 10 with 256K L2 Cache Data Sheet

1 Introduction

This document is a supplementary data sheet to the *AMD Athlon™ Processor Model 10 Data Sheet*, order# 26237 and describes the unique electrical characteristics and ordering information of this processor.

For electrical and other information not specified in this document, see the *AMD Athlon™ Processor Model 10 Data Sheet*, order# 26237, or the *AMD Athlon™ Processor-Based Motherboard Design Guide,* order# 24363.

2 Electrical and Thermal Data

The following section describes the electrical and thermal characteristics unique to this processor.

2.1 Electrical and Thermal Specifications

Table 1 shows the electrical specifications and thermal design power of this processor in the C0 Working state and the S1 Stop Grant state.

Table 1. Electrical and Thermal Specifications for the AMD Athlon™ XP Processor Model 10 with 256K L2 Cache

Frequency in MHz (Model Number)	V_{CC_CORE} (Core Voltage)	I_{CC} (Processor Current)				Thermal Power[4]		Maximum Die Temperature
		Working State C0		Stop Grant S1[1, 2, 3]				
		Maximum	Typical	Maximum	Typical	Maximum	Typical	
1667 (2000+)	1.60 V	37.7 A	29.6 A	8.1 A	4.9 A	60.3 W	47.4 W	90°C
1800 (2200+)	1.60 V	39.3 A	30.9 A	8.1 A	4.9 A	62.8 W	49.4 W	85°C
2000 (2400+)	1.65 V	41.4 A	32.5 A	8.9 A	5.4 A	68.3 W	53.7 W	85°C

Notes:

1. *The maximum Stop Grant currents are absolute worst case currents for parts that may yield from the worst case corner of the process and are not representative of the typical Stop Grant current that is currently about one-third of the maximum specified current.*
2. *These currents occur when the AMD Athlon™ system bus is disconnected and has a low power ratio of 1/8 for Stop Grant disconnect and a low power ratio of 1/8 Halt disconnect applied to the core clock grid of the processor as dictated by a value of 2003_1223h programmed into the Clock Control (CLK_Ctl) MSR. For more information, refer to the* AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656.*
3. *The Stop Grant current consumption is characterized at 50°C and not tested.*
4. *Thermal design power represents the maximum sustained power dissipated while executing publicly-available software or instruction sequences under normal system operation at nominal V_{CC_CORE}. Thermal solutions must monitor the temperature of the processor to prevent the processor from exceeding its maximum die temperature.*

Table 2 shows the electrical specifications and thermal design power of the V_{CC_CORE} = 1.50 V processor in the C0 Working state and the S1 Stop Grant state.

Table 2. Electrical and Thermal Specifications for the AMD Athlon™ XP Processor Model 10 with 256K L2 Cache with V_{CC_CORE} = 1.50 V

Frequency in MHz (Model Number)	V_{CC_CORE} (Core Voltage)	I_{CC} (Processor Current)				Thermal Power[4]		Maximum Die Temperature
		Working State C0		Stop Grant S1[1, 2, 3]				
		Maximum	Typical	Maximum	Typical	Maximum	Typical	
1667 (2000+)	1.50 V	40.2 A	32.9 A	8.1 A	4.9 A	60.3 W	49.3 W	90°C
1800 (2200+)		41.7 A	34.7 A	8.1 A	4.9 A	62.8 W	52.0 W	85°C

Notes:

5. *The maximum Stop Grant currents are absolute worst case currents for parts that may yield from the worst case corner of the process and are not representative of the typical Stop Grant current that is currently about one-third of the maximum specified current.*
6. *These currents occur when the AMD Athlon™ system bus is disconnected and has a low power ratio of 1/8 for Stop Grant disconnect and a low power ratio of 1/8 Halt disconnect applied to the core clock grid of the processor as dictated by a value of 2003_1223h programmed into the Clock Control (CLK_Ctl) MSR. For more information, refer to the* AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656.*
7. *The Stop Grant current consumption is characterized at 50°C and not tested.*
8. *Thermal design power represents the maximum sustained power dissipated while executing publicly-available software or instruction sequences under normal system operation at nominal V_{CC_CORE}. Thermal solutions must monitor the temperature of the processor to prevent the processor from exceeding its maximum die temperature.*

For general information about thermal design for this processor, including layout and airflow considerations, see the *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794, and the cooling guidelines on *http://www.amd.com*.

2.2 V_{CC_CORE} Characteristics

Table 3 shows the AC and DC characteristics for V_{CC_CORE}. See Figure 1 on page 5 for a graphical representation of the V_{CC_CORE} waveform.

Table 3. V_{CC_CORE} AC and DC Characteristics

Symbol	Parameter	Limit in Working State	Units
$V_{CC\_CORE\_DC\_MAX}$	Maximum static voltage above $V_{CC\_CORE\_NOM}$*	50	mV
$V_{CC\_CORE\_DC\_MIN}$	Maximum static voltage below $V_{CC\_CORE\_NOM}$*	–50	mV
$V_{CC\_CORE\_AC\_MAX}$	Maximum excursion above $V_{CC\_CORE\_NOM}$*	150	mV
$V_{CC\_CORE\_AC\_MIN}$	Maximum excursion below $V_{CC\_CORE\_NOM}$*	–100	mV
t_{MAX_AC}	Maximum excursion time for AC transients	10	µs
t_{MIN_AC}	Negative excursion time for AC transients	5	µs

Note:
**All voltage measurements are taken differentially at the COREFB/COREFB# pins.*

Figure 1 shows the processor core voltage (V_{CC_CORE}) waveform response to perturbation. The t_{MIN_AC} (negative AC transient excursion time) and t_{MAX_AC} (positive AC transient excursion time) represent the maximum allowable time below or above the DC tolerance thresholds.

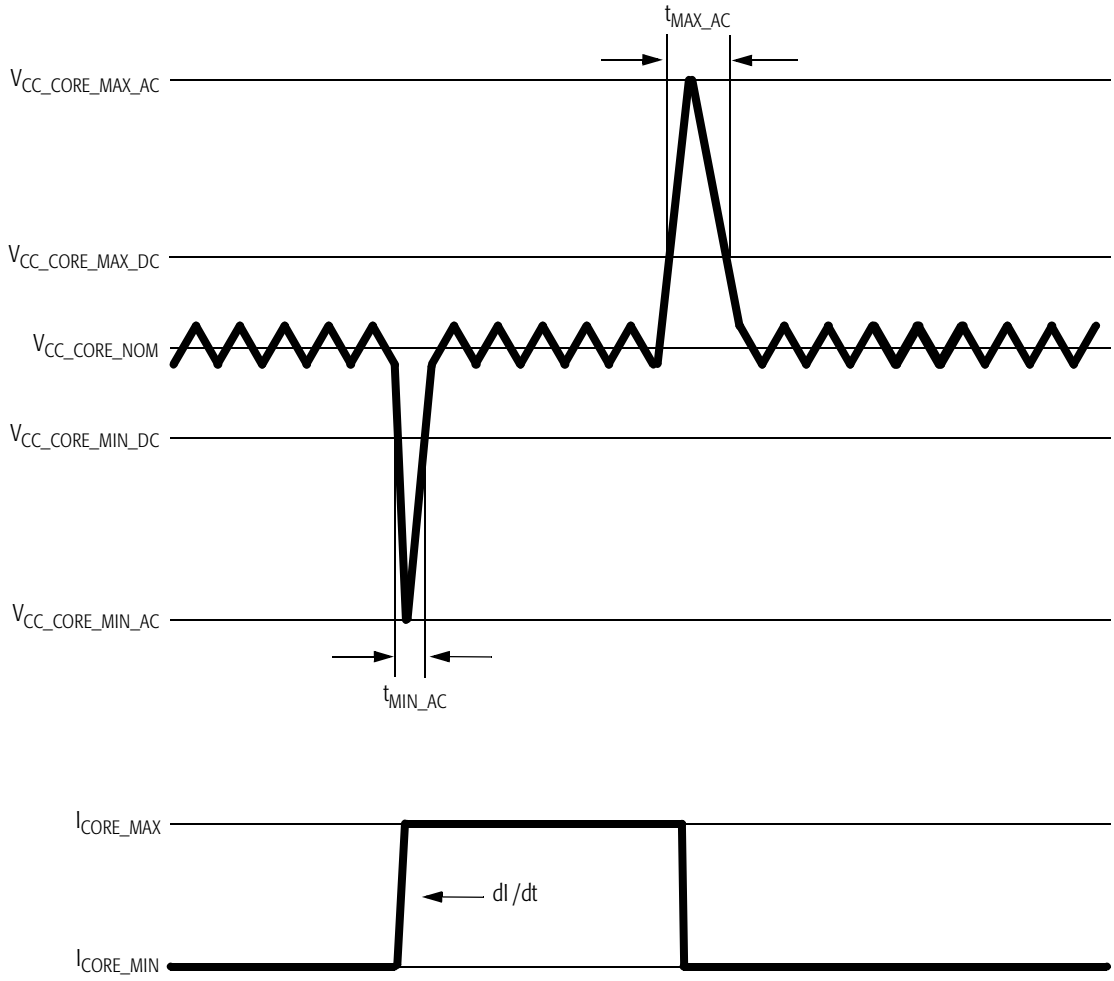


Figure 1. V_{CC_CORE} Voltage Waveform

2.3 SYSCLK and SYSCLK# AC Characteristics

Table 4 shows the SYSCLK/SYSCLK# differential clock AC characteristics of this processor.

Table 4. SYSCLK and SYSCLK# AC Characteristics

Symbol	Parameter Description	Minimum	Maximum	Units	Notes
	Clock Frequency	50	133	MHz	1
	Duty Cycle	30%	70%		
t_1	Period	7.5		ns	2, 3
t_2	High Time	1.05		ns	
t_3	Low Time	1.05		ns	
t_4	Fall Time		2	ns	
t_5	Rise Time		2	ns	
	Period Stability		± 300	ps	

Notes:

1. *The AMD Athlon™ system bus operates at twice this clock frequency.*
2. *Circuitry driving the AMD Athlon system bus clock inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The –20dB attenuation point, as measured into a 20- or 30-pF load must be less than 500 kHz.*
3. *Circuitry driving the AMD Athlon processor system bus clock inputs may purposely alter the AMD Athlon processor system bus clock frequency (spread spectrum clock generators). In no cases can the AMD Athlon processor system bus period violate the minimum specification above. AMD Athlon processor system bus clock inputs can vary from 100% of the specified frequency to 99% of the specified frequency at a maximum rate of 100 kHz.*

Figure 2 shows a sample waveform of the SYSCLK signal.

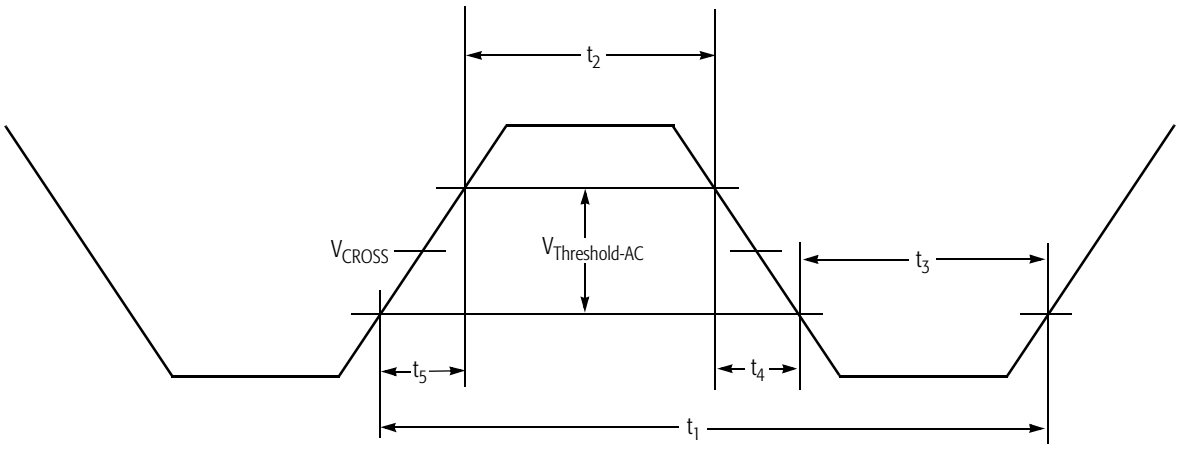


Figure 2. SYSCLK Waveform

2.4 AMD Athlon™ Processor System Bus AC and DC Characteristics

This sections provides the AC and DC characterisitics of the AMD Athlon processor system bus used by this processor.

The AC characteristics of the AMD Athlon processor system bus are shown in Table 5. The parameters are grouped based on the source or destination of the signals involved.

Table 5. AMD Athlon™ Processor System Bus AC Characteristics

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	T_{RISE}	Output Rise Slew Rate	1	3	V/ns	1
	T_{FALL}	Output Fall Slew Rate	1	5	V/ns	1
Forward Clocks	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge	–	385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	770		
	T_{SU}	Input Data Setup Time	300		ps	3
	T_{HD}	Input Data Hold Time	300		ps	3
	C_{IN}	Capacitance on input clocks	4	25	pF	
	C_{OUT}	Capacitance on output clocks	4	12	pF	
Sync	T_{VAL}	RSTCLK to Output Valid	250	2000	ps	4, 5
	T_{SU}	Setup to RSTCLK	500		ps	4, 6
	T_{HD}	Hold from RSTCLK	1000		ps	4, 6

Notes:

1. *Rise and fall time ranges are guidelines over which the I/O has been characterized.*
2. *$T_{SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.*
3. *Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.*
4. *The synchronous signals include PROCRDY, CONNECT, and CLKFWDRST.*
5. *T_{VAL} is the RSTCLK rising edge to the output valid for PROCRDY. The test Load is 25 pF.*
6. *T_{SU} is a setup of CONNECT/CLKFWDRST to the rising edge of RSTCLK. T_{HD} is a hold of CONNECT/CLKFWDRST from the rising edge of RSTCLK.*

Table 6 shows the DC characteristics of the AMD Athlon system bus used by this processor.

Table 6. AMD Athlon™ System Bus DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{REF}	DC Input Reference Voltage		$(0.5 \times V_{CC\_CORE})$ −50	$(0.5 \times V_{CC\_CORE})$ +50	mV	1
$I_{VREF\_LEAK\_P}$	V_{REF} Tristate Leakage Pullup	$V_{IN} = V_{REF}$ Nominal	−100		µA	
$I_{VREF\_LEAK\_N}$	V_{REF} Tristate Leakage Pulldown	$V_{IN} = V_{REF}$ Nominal		100	µA	
V_{IH}	Input High Voltage		V_{REF} +200	V_{CC_CORE} +500	mV	
V_{IL}	Input Low Voltage		−500	V_{REF} −200	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	−1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	$V_{IN} = V_{CC\_CORE}$ Nominal		1	mA	
C_{IN}	Input Pin Capacitance		4	7	pF	
R_{ON}	Output Resistance		$0.90 \times R_{setN,P}$	$1.1 \times R_{setN,P}$	Ω	2
R_{setP}	Impedance Set Point, P Channel		40	70	Ω	2
R_{setN}	Impedance Set Point, N Channel		40	70	Ω	2

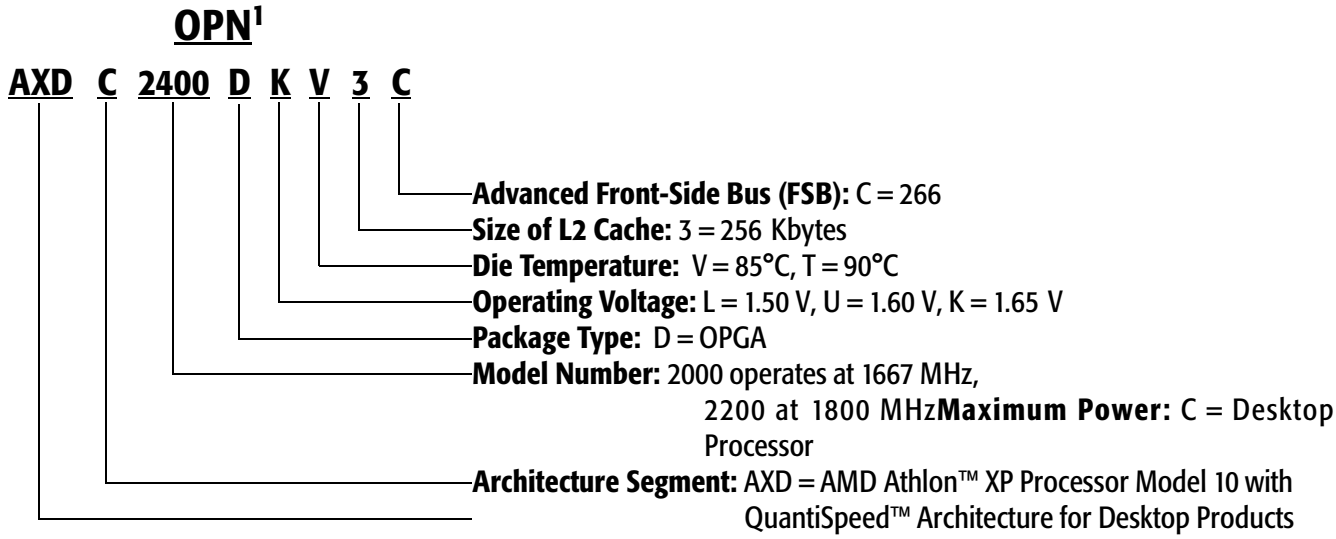
Notes:

1. *V_{REF} is nominally set to 50% of V_{CC_CORE} with actual values that are specific to motherboard design implementation. V_{REF} must be created with a sufficiently accurate DC source and a sufficiently quiet AC response to adhere to the ± 50 mV specification listed above.*
2. *Measured at V_{CC_CORE} / 2.*

3 Ordering Information

Standard AMD Athlon™ XP Processor Model 10 Products

This AMD standard product is available in the operating ranges shown below. The ordering part number (OPN) is formed by a combination of the elements, as shown in Figure 3.



Note:
1. Spaces are added to the number shown above for viewing clarity only.

Figure 3. OPN of the AMD Athlon™ XP Processor Model 10 with 256K L2 Cache